If the Digital Input Board is programmed to detect COS on both rising and falling edges, the minimum time in each state is 2ms. Thus, 4ms is the minimum period of a continuous input signal.

Each input channel is independent and is processed separately, so activity on one channel has no effect on other channels. A COS on one channel can be detected and stored while the debouncer is timing on another channel. Since all inputs are latched simultaneously every millisecond and they are processed separately, there can be minimum of 1 ms between events that occur on different channels.

Change-of-State Detection

State change detection can be programmed for rising edge (low-to-high transition), falling edge (high-to-low transition), or both rising and falling edges. In addition, COS detection can generate an interrupt or be disabled.

Time Tagging

Each Change-of-State event can be time tagged with a timer value of 0 to 65 seconds and is initialized or preset by writing to the time tag register.

The timer value is updated every millisecond. When the timer value has reached its maximum value, it rolls over to 0 and notifies the host of a time tag rollover via a bit in the Control Register, or if desired, an interrupt may be issued.

Sequence-of-Events

Each Change-of-State (depending on change select options) can be time-tagged in the sequence-of-event buffer. The SOE buffer collects the channel ID, and the time (time tag register) in which the state changed. This buffer can contain 3,000 events. When the host is accessing the SOE buffer, the Digital Input Board will continue to monitor the inputs and store events in a mirrored SOE buffer. The additional buffer also provides 3,000 events of storage. This allows the user the ability to process the SOE data (without time constraint problems) and not lose any event data. The SOE logic can provide an interrupt to the host at the End-of-Buffer or an interrupt at a count provided by the user (programmable).

Pulse Accumulation

Each channel has an associated Pulse Accumulation Count (PAC) register. These registers have values which represent the number of pulses which have been detected at the field input. A pulse is edge-recognized by either a state change from a 0 to 1 or a state change from 1 to 0. The user will be notified when the count in the PAC register has reached its maximum value of 65,535 pulses. This condition is indicated by a flag set in the Control Register, or if desired, an interrupt may also be issued.

Inputs

The Digital Input Board is a Voltage Sensing board. The input configurations for Voltage Sensing are shown in Figure 2. Voltage Sensing does not provide pull-ups resistors.

The electrical specifications for the inputs are shown in Table 1 below.

Table 1. Electrical Specifications

Input Voltage	Threshold High (V)	Threshold Low (V)	Voltage Sensing (mA)
			Source Current @ V_{input} ± 15%
24VDC 125VDC	17 85	6.0 30.0	.8 .7

Functional Characteristics

Interchannel Crosstalk Rejection: 80dB minimum at 1kHz

Common-Mode Rejection (CMRR): 80dB minimum DC to 60Hz

Isolation: 1,500VDC or 1,100VRMS field-to-bus, channel-to-channel for voltage sensing.

VMEbus Compliance: This board complies with the VMEbus specification (ANSI/IEEE STD 1014-1987 IEC 821 and 297) with the following mnemonics:

Addressing Mode	Responding Address Modifiers
A24	$39 (Standard nonprivileged data access) or $3D (Standard supervisory data access)
A16	$29 (Short nonprivileged I/O access) or $2D (Short supervisory I/O access)
Data Access:	D16, D08(EO)
Interrupts:	One, any level, ROAK

Board Address: The base VMEbus address is set by configuration of a jumper field. A jumper exists for each of the addresses A23 through A14; thus, the address space occupied by this board is 8k words.

VMEbus Access: The Address Modifier is jumper selectable for nonprivileged, supervisory or both board accesses.

Self-Test: Self-test is run automatically after a system reset, and can also be run by activating the Test Mode bit in the CSR. A pass/fail value is stored in the Control Register space. The LED remains illuminated regardless of the pass/fail status of the self-test. The self-test is primarily an integrity check of the microcontroller and the on-board memory.

System Reset: After a system reset, the following default conditions exist:

Input transfers with 1ms debounce

LED illuminated

Test Mode enabled

Front Panel Status LED: This indicator is illuminated after a system reset. The LED can also be turned ON and OFF under software control.

Interrupts: An interrupt can be issued on any level (software selectable) and a single byte vector will be placed on the bus when acknowledged. There is one ROAK interrupt for the board. The following conditions can initiate the interrupt:

COS on any of the 64 channels

Time-Tag Rollover

Pulse Accumulation Rollover on any of the 64 channels

Sequence-of-Event, End-of-buffer

Sequence-of-Event buffer count equal to programmable maximum count provided by user

Each of these interrupt conditions may be enabled or disabled by the host.

Physical/Environmental

Dimensions: Standard VME double height board (160 x 233.5mm)

Temperature: 0 to +65°C, operating
-25 to +85°C, storage

Relative Humidity: 20 to 80%, noncondensing

Cooling: Forced air

Power Requirements: 2.0A (typical) at 5V plus any power dissipated in pull-up resistors

Altitude: Operation to 10,000ft (3,048m)

Weight (Mass): 0.7kg maximum

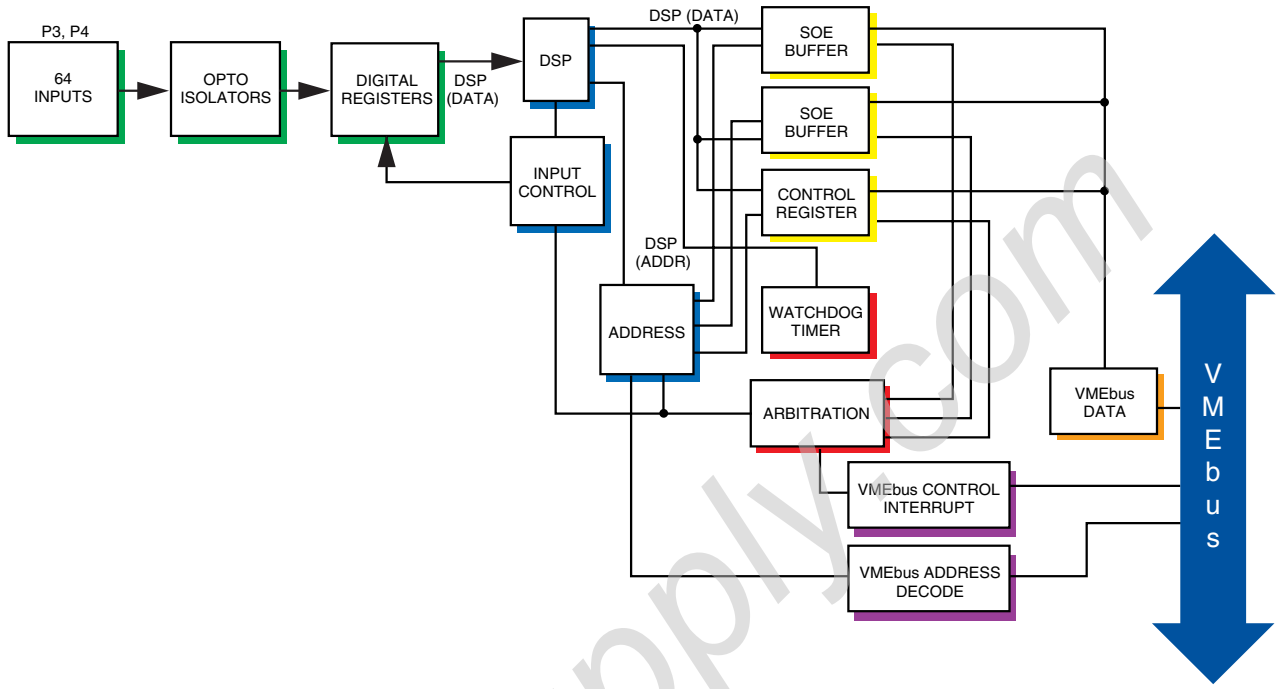

Figure 1. Functional Block Diagram

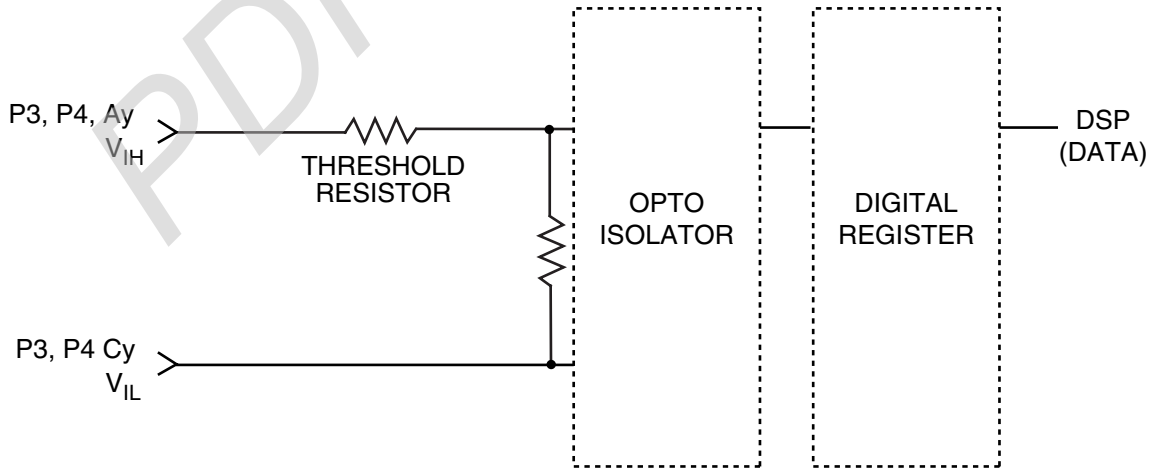

Figure 2. User Input Connection Circuit (Voltage Sensing)