Quad/Dual Channel Incremental Encoder Interface

GE Fanuc Automation

Programmable Control Products

PCB Bus Series – Dual and Quad Channel Incremental Encoder Interface

User's Manual

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Warnings, Cautions, and Notes as Used in this Publication

Warning

Warning notices are used in this publication to emphasize that hazardous voltages, currents, temperatures, or other conditions that could cause personal injury exist in this equipment or may be associated with its use.

In situations where inattention could cause either personal injury or damage to equipment, a Warning notice is used.

Caution

Caution notices are used where equipment might be damaged if care is not taken.

Note

Notes merely call attention to information that is especially significant to understanding and operating the equipment.

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Content of this Manual

This manual applies to the following Incremental Encoder Interface models

PCB-3695-0 PCB-3795-0

Related Publications

Additional information about Motion solutions is available at
http://www.gefanuc.com/support/plc/m-MotionSolutions.htm.

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SECTION 1.0

GENERAL DESCRIPTION

1.1 INTRODUCTION

The Whedco IBM Bus Series Incremental Encoder Interface makes position feedback with an incremental encoder simple and reliable. Two versions are available - Dual and Quad. The Dual Channel Encoder Interface has two independent encoder channels and the Quad Channel Encoder Interface has four independent encoder channels. Each channel accepts quadrature and index pulse input signals from an encoder. Four parallel outputs per channel are available for set point triggers. In addition, the starting reference position may be initialized to any given value within the counting range. Home position may also be specified at the user's discretion as the occurrence of the index pulse, a home limit switch input, or as the occurrence of the two in tandem.

The interface is completely self-contained and supervises the entire counting and conversion routine after receiving command instructions from the host CPU. Position data is stored on-board until requested by the host.

1.2 FEATURES

Complete signal conversion and conditioning for two or four independent channels of incremental encoder interface.

Resident microprocessor and proprietary firmware supervise counting and conversion routines, thus minimizing time requirements on the host CPU.

Accommodates single-ended or differential inputs up to +/- 15 VDC.

Tracks accumulated position to 4,294,967,296 pulses or +/- 2,147,483,648.

Four set points per channel can be programmed as active when the position counters are less than or greater than the set point position or within a range between two positions; each set point can be individually configured as an interrupt over the bus or to trigger a parallel output from the card.

Position pulse multiplier provides for position resolution one, two, or four times greater than encoder line density.

SECTION 2.0

INSTALLATION

2.1 INSPECTION

Before installing or applying power to the card, visually inspect it and assert that there is no shipping damage. If, by chance, any I.C. has been shaken out of its socket in transit, reinsert the loose leads into the socket.

2.2 MAPPING

The encoder interface occupies 32 consecutive I/O addresses. Port assignment is D.I.P. switch programmable to any 32 byte boundary. The card is shipped from the factory at port addresses 300h through 31Fh. The I/O ports can be changed using D.I.P switch SW1 located near the 62 pin edge connector. Refer to Table 2-1 to select the switch setting for the I/O addresses desired. Note that only Positions 1, 2, 3, 4, and 5 set I/O port addresses, Positions 6 and 7 are unused.

Table 2-1 I/O Map D.I.P. Switch Setting (SW1)

BOUNDARY STARTING ADDRESS	POSITIONS 1 2 3 4 5
000h	0 0 0 0 0
020h	1 0 0 0 0
040h	0 1 0 0 0
060h	1 1 0 0 0
080h	0 0 1 0 0
0A0h	1 0 1 0 0
0C0h	0 1 1 0 0
0E0h	1 1 1 0 0
100h	0 0 0 1 0
120h	1 0 0 1 0
140h	0 1 0 1 0
160h	1 1 0 1 0
180h	0 0 1 1 0
1A0h	1 0 1 1 0
1C0h	0 1 1 1 0
1E0h	1 1 1 1 0
200h	0 0 0 0 1
220h	1 0 0 0 1
240h	0 1 0 0 1
260h	1 1 0 0 1
280h	0 0 1 0 1
2A0h	1 0 1 0 1
2C0h	0 1 1 0 1
2E0h	1 1 1 0 1
300h	0 0 0 1 1
320h	1 0 0 1 1
340h	0 1 0 1 1
360h	1 1 0 1 1
380h	0 0 1 1 1
3A0h	1 0 1 1 1
3C0h	0 1 1 1 1
3E0h	1 1 1 1 1

"0" = switch position closed-------
"1" = switch position open---------

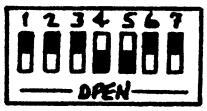


Illustration shows setting for port addresses 300h through 31Fh. Darkened area indicates side of switch depressed.

2.3 INCREMENTAL ENCODER CONNECTIONS

The encoder interface provides input lines for single-ended or differential output encoders as well as a power output line for 5 and 12 volt encoders. 15 volt encoders will require an external power supply. The index line can be optionally connected provided the encoder is so equipped.

To connect the encoders, simply follow the diagrams given in Figures 2-1, 2-2, 2-3, and 2-4. Keep in mind that shorting plugs must be installed in jumpers JP1, JP2, and JP3 for channel one, jumpers JP4, JP5, and JP6 for channel two, jumpers JP13, JP14, and JP15 for channel three, and jumpers JP16, JP17, and JP18 for channel four when using single-ended encoders and removed when using differential. Refer to Appendix E for the location of the jumpers. The card comes shipped with the shorting plugs installed.

The encoder interface comes with two LEDs per channel which indicate the direction in which the encoder is turning. When turning in the positive direction, the corresponding green LED lights. When turning in the negative direction, the corresponding yellow LED lights. These LEDs are helpful in determining that the encoders are working properly and that the polarity of the encoder connections are correct.

Figure 2-1 Interfacing to a Single-Ended Encoder without an External Power Supply

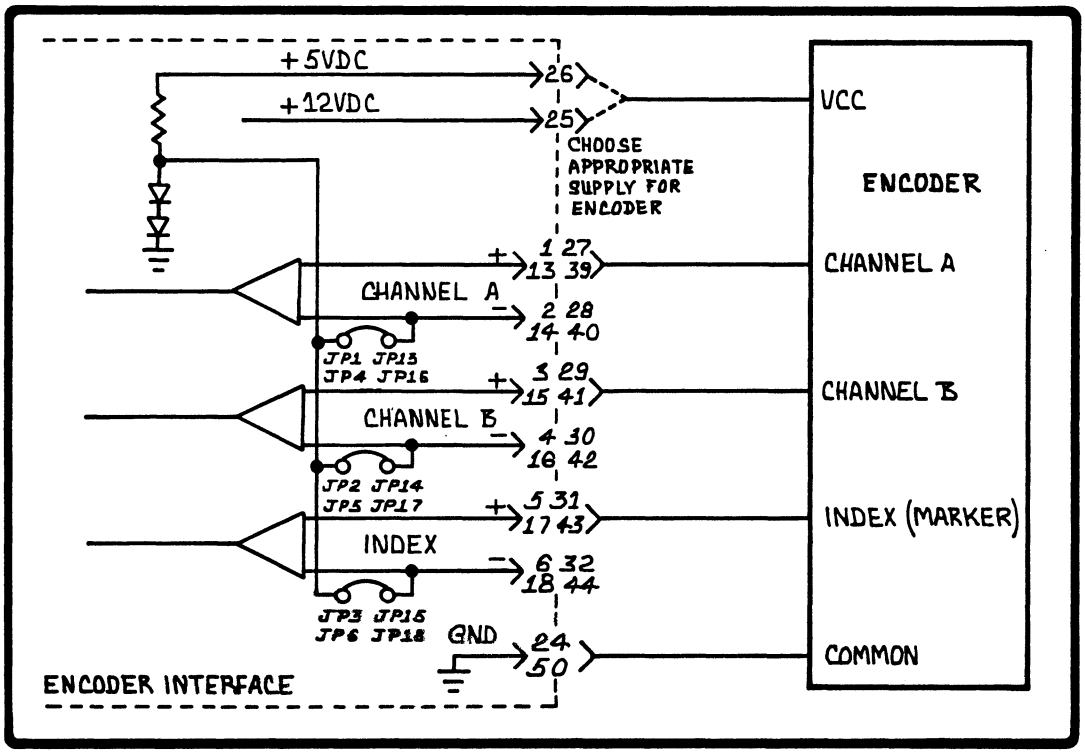


Figure 2-2 Interfacing to a Single Ended Encoder with an External Power Supply

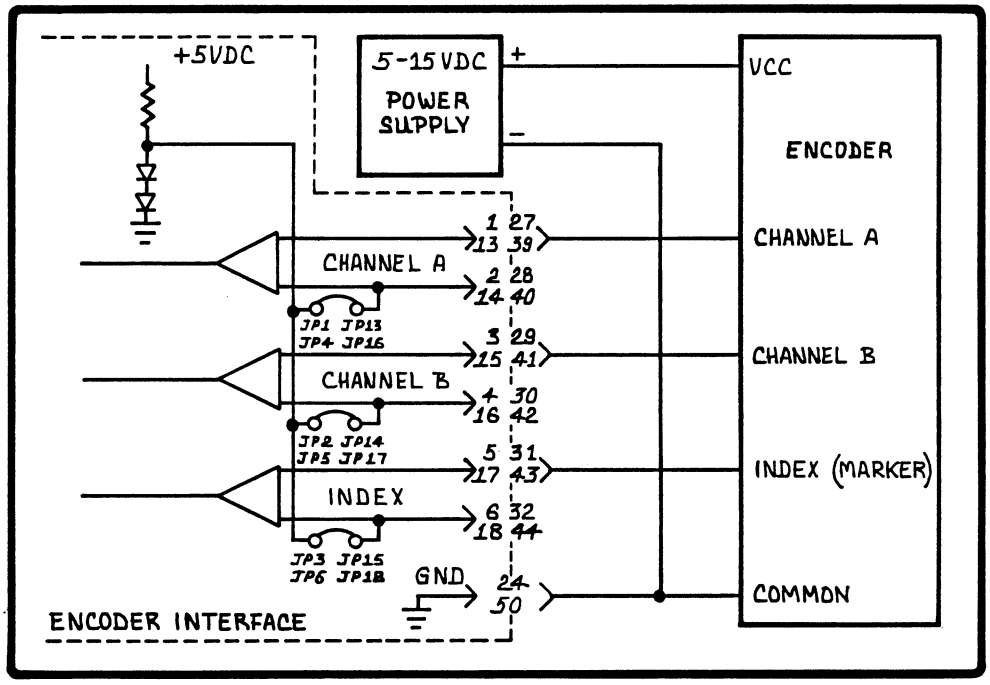


Figure 2-3 Interfacing to a Differential Encoder without an External Power Supply

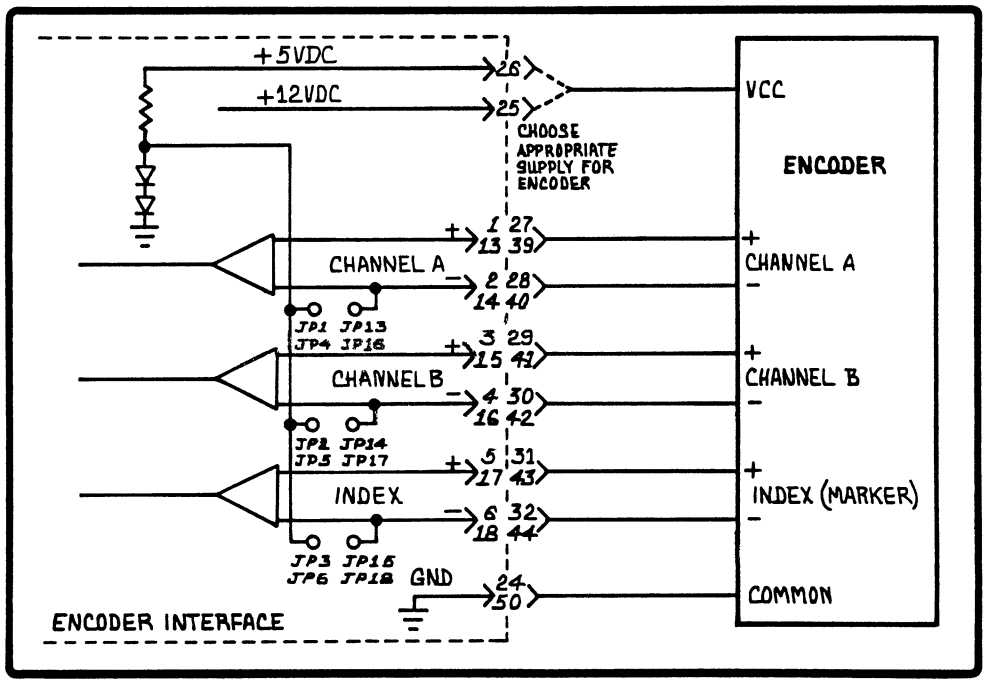
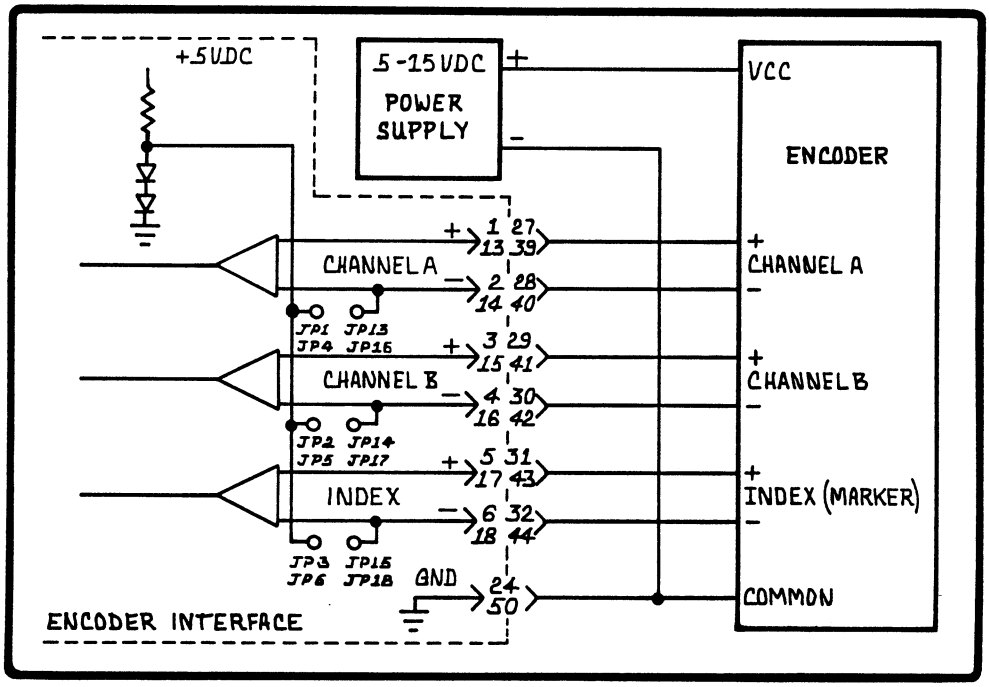


Figure 2-4 Interfacing to a Differential Encoder with an External Power Supply



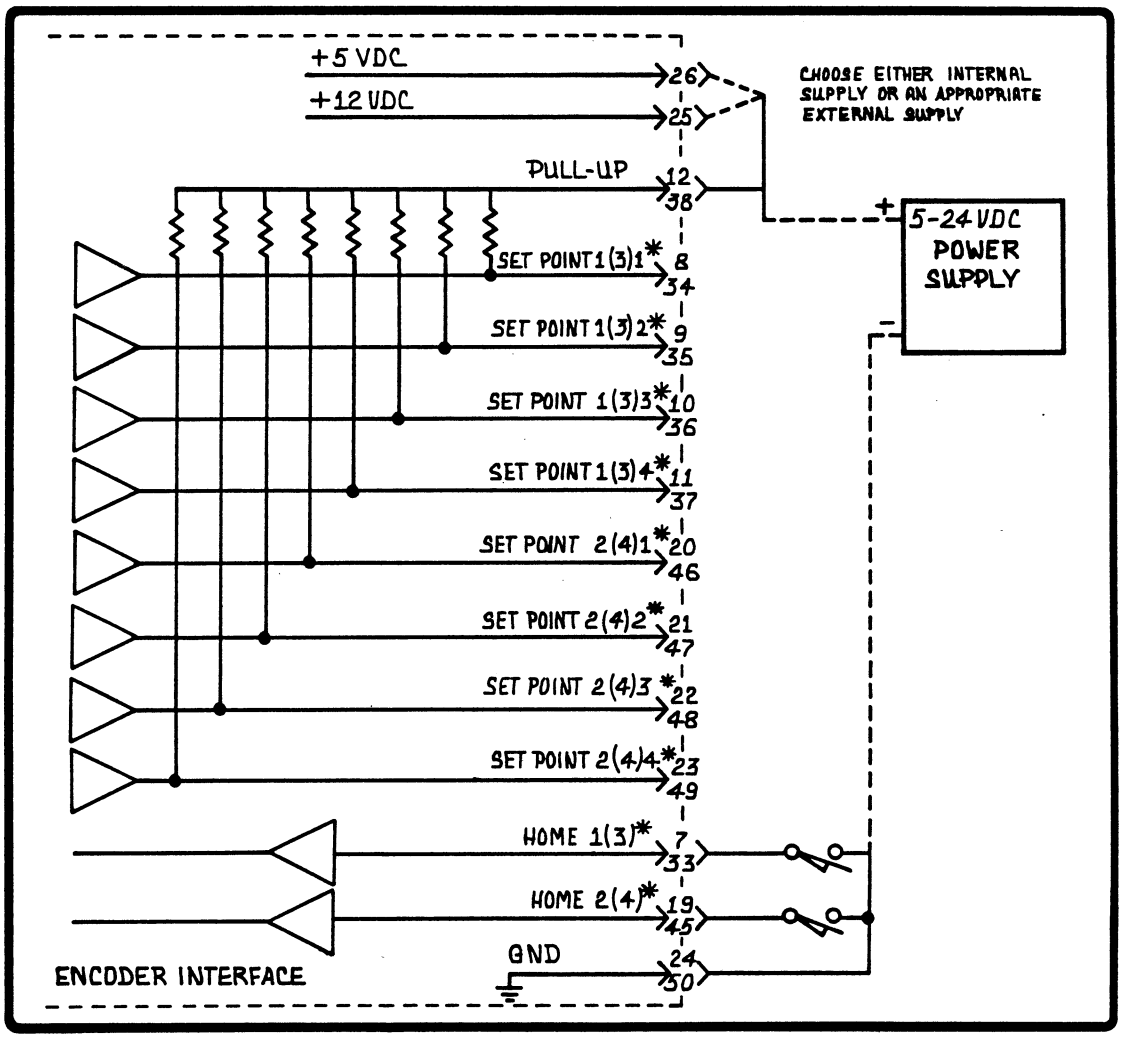
2.4 CONFIGURING INTERRUPTS

The encoder interface supports interrupts on interrupt lines IRQ2 through IRQ7. The particular interrupt line desired is selected by installing a shorting plug on the appropriate jumper - JP7 for IRQ2, JP8 for IRQ3, through JP12 for IRQ7. Refer to Appendix E for the location of the jumpers. The card is shipped with the shorting plug on JP8 for IRQ3.

2.5 I/O LINES

The encoder interface provides a home input line and 4 set point output lines per channel. For a pin out of the I/O connector, see Appendix A, Section A.3. The home input lines are active low and can accept voltages up to 15 vdc. The output lines are active low also. They are sinking outputs and will sink up to 125mA at up to 24 volts. The Pull-Up line should be connected to the interface voltage used. The 5 or 12 volt supply line can be used if appropriate. For a connection diagram, see Figure 2-5.

Figure 2-5 Typical Connection of I/O Lines



"*" = Signal is active low.

SECTION 3.0

OPERATION

3.1 READING FROM AND WRITING TO THE I/O REGISTERS

The encoder interface has 32 registers through which it communicates with the host CPU. These 32 registers are divided into two sets of 16 registers each which perform exactly the same functions. The first set of 16 registers is used for channels one and two and the second set is used for channels three and four. In a set of 16 registers, eight registers hold the two 32 bit position counters for the two channels. Four registers transfer data back and forth. One provides the position handshake. One holds the status of the set points. One contains the status of the encoder interface for the two channels, and one is used to give the interface commands for the two channels. The assignment of the I/O registers to the port locations is given in Table 3-1.

Table 3-1 I/O Register Assignment

X00	low
X01	Channel 1 Position
X02	
X03	high
X04	low
X05	Channel 2 Position
X06	
X07	high
X08	low
X09	Data for Channels 1 & 2
X0A	
X0B	high
X0C	Position Handshake for Channels 1 & 2
X0D	Set Points of Channels 1 & 2
X0E	Status of Channels 1 & 2
X0F	Command register for Channels 1 & 2
X10	low
X11	Channel 3 Position
X12	
X13	high
X14	low
X15	Channel 4 Position
X16	
X17	high
X18	low
X19	Data for Channels 3 & 4
X1A	
X1B	high
X1C	Position Handshake for Channels 3 & 4
X1D	Set Points of Channels 3 & 4
X1E	Status of Channels 3 & 4
X1F	Command register for Channels 3 & 4

"X" = base address (see Section 2.2)

Any of the 32 I/O registers may be written to or read by the host CPU at any time except for the Command Registers which should only be written to when their most significant bit (bit 7) is set. This is their Ready for Command Bit. The encoder interface causes the host to wait in response to a write or read to the I/O registers until the current on-board bus cycle is completed. This means a typical wait of 0.2 - 1.4 microseconds.

The host access disables the interface CPU (puts the Z-80 into the DMA mode) during the host read or write. This causes no problem as long as the accesses are not more than 25% of the interface CPU's time or a regular basis of not more than one every 32 microseconds. Therefore, exercise caution when writing tight loops which wait for one of the flags to change state. If the system CPU accesses too often, the interface CPU may not be able to keep up with the incoming encoder pulses and lose some of them.

3.2 OPERATING STATUS

The encoder interface has two Status Registers which provide information on the operation of the card. One of the registers is for channels one and two and the other is for channels three and four. Table 3-2 lists the bits in the registers and the purpose of each.

Table 3-2 Status Registers Bits

BIT	LABEL	DESCRIPTION
B0	CHNL. 1(3) HOME	This bit reflects the status of channel 1(3) home input. 1 = input low (active)
B1	CHNL. 1(3) INDEX	This bit reflects the status of channel 1(3) index pulse. 1 = input high (active)
B2	CHNL. 1(3) OVERFLOW	If channel 1(3) Position Register over- or under-flows, this bit becomes true. It can be reset by using the Clear Channel 1(3) Overflow Command (09h).
B3	CHNL. 2(4) HOME	This bit reflects the status of channel 2(4) home input. 1 = input low (active)
B4	CHNL. 2(4) INDEX	This bit reflects the status of channel 2(4) index pulse. 1 = input high (active)
B5	CHNL. 2(4) OVERFLOW	If channel 2(4) Position Register over- or under-flows, this bit becomes true. It can be reset by using the Clear Channel 2(4) Overflow Command (19h).
B6	INTERRUPT REQUEST	This bit is true whenever the card has the interrupt request line active for 1 or 2(3 or 4).
B7	POSITION AVAILABLE	When this bit is true, the card is not updating the Position Registers for 1 & 2(3 & 4) which makes the registers available to be read.

Note: If bit = 1, then condition is true

3.3 READING POSITION

To avoid the possibility of getting contaminated data, a particular handshake procedure should be used when reading the Position Registers. This procedure is as follows:

1) Set the Request Position Bit (bit 0) of the appropriate Position Handshake Register to one.
2) Wait for the Position Available Bit (bit 7) of the appropriate Status Register to be one.
3) Read the Position Registers.
4) Reset the Request Position Bit to zero.

It is important to always perform the last step since the encoder interface will not update the Position Registers when the Request Position Bit is true.

SECTION 4.0

PROGRAMMING

4.1 INTRODUCTION

To program the IBM Bus Series Incremental Encoder Interface, the host CPU writes commands to the appropriate command port. This is done by first waiting for the most significant bit (bit 7) of the command port to be true. This is the Ready for Command Bit. After this bit is high, the appropriate data port should be loaded with any pertinent information needed for the command and then the particular command should be written to the appropriate command port.

After the encoder interface has been programmed, the host CPU can periodically read the appropriate status and set point ports to check up on the encoders or it can wait to be interrupted. In addition, at any time, the host CPU can read the 32 bit position counters for each channel by making use of the position handshake procedure discussed in Section 3.3.

4.2 PARAMETERS

Two parameters define operation of the counters which need to be loaded after power up or after a software reset command. The first, Position Pulse Multiplier, determines how many pulses should be counted for each line on the encoder. Its valid values are "1" for one count per line (default), "2" for two counts per line, or "4" for four counts per line. The command to load it is 10 (0Ah) for Channel One(Three) and 26 (1Ah) for Channel Two(Four).

The second parameter is Position Range Type. When this parameter is 0, the range of the counter is from 0 to 4,294,967,296. When the parameter is 1 (default), the range of the counter is from -2,147,483,648 to 2,147,483,647 in 2's complement notation. The command to load it is 11 (0Bh) for Channel One(Three) and 27 (1Bh) for Channel Two(Four).

4.3 SETTING POSITION

Upon power up or after a software reset, the position counters are set to the middle of their ranges which are 2,147,483,648 for the unsigned range and 0 for the signed range. To change the position, at any time, the Set Position Command is used. This command has several modifiers associated with it to select which channel's counter to set, when to perform the set, and to what value the counter should be set. See Table 4-1 for a listing of the command byte needed for each type of position set.

Table 4-1 Command Byte for Specified Position Sets

TYPE OF POSITION SET	COMMAND (HEX)	(DECIMAL)
Channel 1(3):		
Immediately set at middle of range	40	64
Immediately set at position in Data Register	41	65
Find home, set at middle of range	44	68
Find home, set at position in Data Register	45	69
Find index, set at middle of range	48	72
Find index, set at position in Data Register	49	73
Find home & index, set at middle of range	4C	76
Find home & index, set at Data Register	4D	77
Channel 2(4):		
Immediately set at middle of range	50	80
Immediately set at position in Data Register	51	81
Find home, set at middle of range	54	84
Find home, set at position in Data Register	55	85
Find index, set at middle of range	58	88
Find index, set at position in Data Register	59	89
Find home & index, set at middle of range	5C	92
Find home & index, set at Data Register	5D	93

4.4 SET POINTS

Each channel has four set points which can be set to any location over the entire range of the position counters. Each has a flag and an output line with which it is associated. The flags are located in the appropriate Set Point Register. Channel 1(3), point 1, is assigned to bit 0; channel 1(3), point 2, to bit 1, and so forth. Channel 2(4) begins with bit 4. The output lines are listed in Appendix A, Table A-1.

These set points can be programmed to be active when the position counters are less than the set point position, when the position counters are greater than the set point position, or when the position counters are between the two set point positions. The set points are programmed by first loading the appropriate Data Register with the set point location and then issuing the appropriate version of the Set Point Command. To program a set point to be active between two positions, the lower position is loaded first by the above method. Then the higher position is loaded with the above method using the same Set Point Command as before. Table 4-2 lists the command for different cases.

Table 4-2 Command Byte for Specific Set Point Cases

SET POINT CASE	COMMAND (HEX)	(DECIMAL)
Channel 1(3):		
Set point 1 enabled when greater than	20	32
Set point 1 enabled when less than	21	33
Set point 1 enabled when between	22	34
Set point 1 turned off	23	35
Set point 2 enabled when greater than	24	36
Set point 2 enabled when less than	25	37
Set point 2 enabled when between	26	38
Set point 2 turned off	27	39
Set point 3 enabled when greater than	28	40
Set point 3 enabled when less than	29	41
Set point 3 enabled when between	2A	42
Set point 3 turned off	2B	43
Set point 4 enabled when greater than	2C	44
Set point 4 enabled when less than	2D	45
Set point 4 enabled when between	2E	46
Set point 4 turned off	2F	47
Channel 2(4):		
Set point 1 enabled when greater than	30	48
Set point 1 enabled when less than	31	49
Set point 1 enabled when between	32	50
Set point 1 turned off	33	51
Set point 2 enabled when greater than	34	52
Set point 2 enabled when less than	35	53
Set point 2 enabled when between	36	54
Set point 2 turned off	37	55
Set point 3 enabled when greater than	38	56
Set point 3 enabled when less than	39	57
Set point 3 enabled when between	3A	58
Set point 3 turned off	3B	59
Set point 4 enabled when greater than	3C	60
Set point 4 enabled when less than	3D	61
Set point 4 enabled when between	3E	62
Set point 4 turned off	3F	63

4.5 INTERRUPTS

Each set point is associated with an Interrupt Bit which can be programmed to interrupt the system processor when its corresponding set point is high, low, makes a low-to-high transition, or makes a high-to-low transition. The Set Interrupt Command sets up the type of interrupt for a set point and its construct is similar to the Set Point Command. Table 4-3 lists the command for different cases.

Table 4-3 Command Byte for Specific Set Interrupt Cases

SET INTERRUPT CASE	COMMAND (HEX)	COMMAND (DECIMAL)
Channel 1(3):		
Set point 1 high to low transition	60	96
Set point 1 low to high transition	61	97
Set point 1 low	62	98
Set point 1 high	63	99
Set point 2 high to low transition	64	100
Set point 2 low to high transition	65	101
Set point 2 low	66	102
Set point 2 high	67	103
Set point 3 high to low transition	68	104
Set point 3 low to high transition	69	105
Set point 3 low	6A	106
Set point 3 high	6B	107
Set point 4 high to low transition	6C	108
Set point 4 low to high transition	6D	109
Set point 4 low	6E	110
Set point 4 high	6F	111
Channel 2(4):		
Set point 1 high to low transition	70	112
Set point 1 low to high transition	71	113
Set point 1 low	72	114
Set point 1 high	73	115
Set point 2 high to low transition	74	116
Set point 2 low to high transition	75	117
Set point 2 low	76	118
Set point 2 high	77	119
Set point 3 high to low transition	78	120
Set point 3 low to high transition	79	121
Set point 3 low	7A	122
Set point 3 high	7B	123
Set point 4 high to low transition	7C	124
Set point 4 low to high transition	7D	125
Set point 4 low	7E	126
Set point 4 high	7F	127

When the host CPU starts running the interrupt service routine, the encoder interface must be polled to find out which set point generated the interrupt. First, the set of channels which generated the interrupt must be determined. This is done by checking the Interrupt Request Bit (bit 6) of the two Status Registers. The set of channels, either 1 & 2 or 3 & 4 which is requesting the interrupt will have its bit set.

After the correct set has been determined, the polling is continued by issuing the Read Interrupt Bits Command to the appropriate Command Register. This command returns an 8 bit value in the low order byte of the appropriate Data Register which is valid when the Ready for Command Bit is true. Each one of the bits in the byte stands for one of the interrupt sources and is true when the bit is one. The order of the bits from LSB to MSB is channel 1(3) - set point 1, channel 1(3) - set point 2, through channel 2(4) - set point 4. This order is also the order of precedence assigned to the different interrupts (i.e. channel 1(3) - set point 1 interrupt will be acknowledged first).

To acknowledge an interrupt, the system CPU should first read the Interrupt Bits to find out which set point caused the interrupt. Then it should use the Interrupt Acknowledge Command which resets the highest priority Interrupt Bit. At this point, the CPU should do whatever is necessary to service the interrupt. See 4.6 for an example of using interrupts.

Table 4-4 lists commands associated with interrupts along with a description of the function of each.

Table 4-4 Interrupt Commands

COMMMAND	NAME	DESCRIPTION
1h	Master Enable Interrupts	Enables all interrupts for 1 & 2(3 & 4)
2h	Master Disable Interrupts	Disables all interrupts for 1 & 2(3 & 4)
3h	Clear Interrupts	Clears all pending interrupts for 1 & 2(3 & 4)
4h	Interrupt Acknowledge	Clears highest priority interrupt for 1 & 2(3 & 4)
5h	Read Interrupt Bits	Returns the 8 Interrupt Bits in the low order byte of the Data Register. These bits are available when the Ready for Command Bit is true.
6h	Enable Channel 1(3) Interrupts	Enables interrupts from Channel 1(3)
7h	Disable Channel 1(3) Interrupts	Disables interrupts from Channel 1(3)
8h	Reset Channel 1(3) Interrupts	Clears all interrupt types set up by the Set Interrupt Command for Channel 1(3)
16h	Enable Channel 2(4) Interrupts	Enables interrupts from Channel 2(4)
17h	Disable Channel 2(4) Interrupts	Disables interrupts from Channel 2(4)
18h	Reset Channel 2(4) Interrupts	Clears all interrupt types set up by the Set Interrupt Command for Channel 2(4)

4.6 PROGRAMMING EXAMPLES

Two examples of programming the card are provided in this section. They are coded in a pseudo code similar to BASIC.

Example 1:

This example shows how to set up and poll a set point using Channel 1. The channel uses the 4 times position pulse multiplier and the unsigned counter range. The set point is placed at 2,147,484,648 and is active when the counter is greater than 2,147,484,648. The flow chart to implement this is given in Figure 4-1, and a program listing is given in Table 4-5.

Figure 4-1 First Programming Example

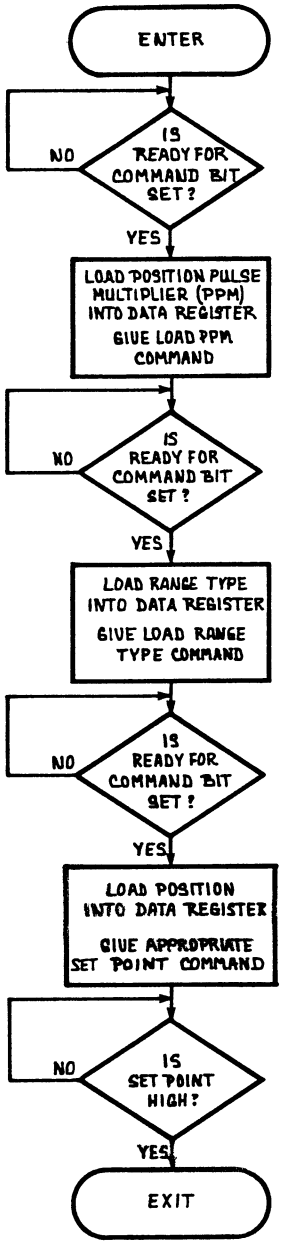


Table 4-5 First Programming Example

```
; This program assumes the card is mapped at ports 300h - 31Fh.

START: IF NOT ( IN(30FH) AND 80H ) GOTO START ; Wait for Ready for Command
                                                ; (RFC) Bit
       OUT(308H,04H)                 ; Load position pulse multiplier (PPM)
       OUT(30FH,0AH)                 ; Give load PPM Command
LOOP1: IF NOT ( IN(30FH) AND 80H ) GOTO LOOP1 ; Wait for RFC Bit
       OUT(308H,00H)                 ; Load range type into Data Register
       OUT(30FH,0BH)                 ; Give Load Range Type Command
LOOP2: IF NOT ( IN(30FH) AND 80H ) GOTO LOOP2 ; Wait for RFC Bit
       OUT(308H,POS1)                ; Load position into Data Register
       OUT(309H,POS1/100H)
       OUT(30AH,POS1/10000H)
       OUT(30BH,POS1/1000000H)
       OUT(30FH,20H)                 ; Give appropriate Set Point Command
LOOP3: IF NOT ( IN(30DH) AND 01H ) GOTO LOOP3 ; Wait for set point
```

Example 2:

This example illustrates the techniques used in setting up an interrupt driven set point instead of polling. In this case, channel 2 - set point 3 is configured to generate an interrupt when the counter goes past 1000. The default position pulse multiplier and the default range type are used. The flow chart is given in Figure 4-2, and a program listing is given in Table 4-6.

Figure 4-2 Second Programming Example

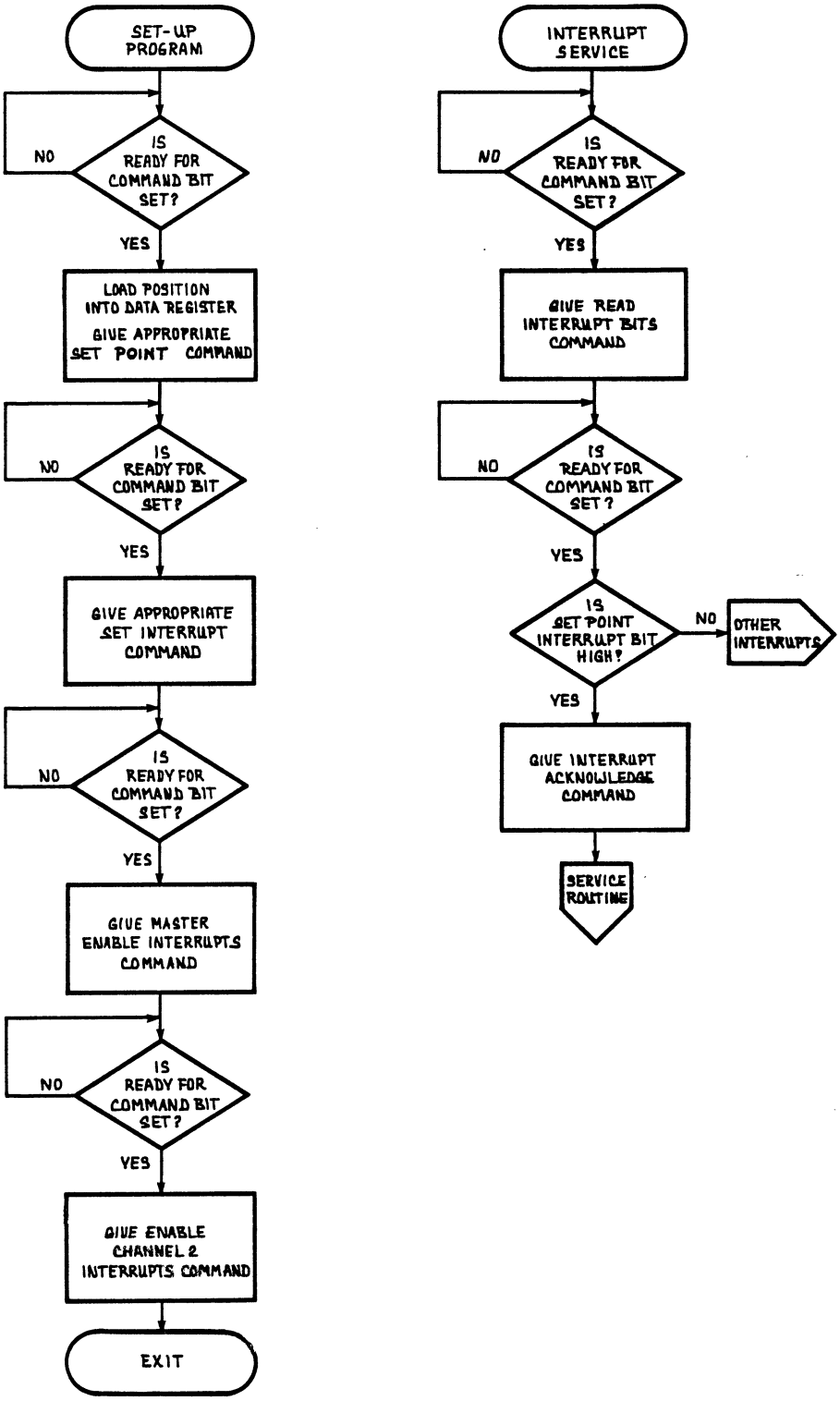


Table 4-6 Second Programming Example

```
; This program assumes the card is mapped at ports 300h - 31Fh.

START: IF NOT ( IN(30FH) AND 80H ) GOTO START ; Wait for Ready for Command
                                              ; (RFC) Bit
       OUT(308H,POS1)                ; Load position into Data Register
       OUT(309H,POS1/100H)
       OUT(30AH,POS1/10000H)
       OUT(30BH,POS1/1000000H)
       OUT(30FH,38H)                 ; Give appropriate Set Point Command
LOOP1: IF NOT ( IN(30FH) AND 80H ) GOTO LOOP1 ; Wait for RFC Bit
       OUT(30FH,79H)                 ; Give appropriate Set Interrupt Com.
LOOP2: IF NOT ( IN(30FH) AND 80H ) GOTO LOOP2 ; Wait for RFC Bit
       OUT(30FH,01H)                 ; Give master enable Interrupts Command
LOOP3: IF NOT ( IN(30FH) AND 80H ) GOTO LOOP3 ; Wait for RFC Bit
       OUT(30FH,16H)                 ; Give enable channel 2 Interrupts Com.

; This is a partial interrupt service routine
INTER: IF NOT ( IN(30FH) AND 80H ) GOTO INTER ; Wait for RFC Bit
       OUT(30FH,05H)                 ; Give read Interrupt Bits Command
LOOP4: IF NOT ( IN(30FH) AND 80H ) GOTO LOOP4 ; Wait for RFC Bit
       IF NOT ( IN(308H) AND 40H ) GOTO ELSEWHERE ; Interrupt was
                                    ; not caused by the set point.
       OUT(30FH,04H)                 ; Give Interrupt Acknowledge Command
; Now whatever needs to be done goes here
```

SECTION 5.0

MAINTENANCE

5.1 TROUBLESHOOTING

If you have trouble with the card, the following flow chart and table should help you out.

Figure 5-1 Troubleshooting Flow Chart

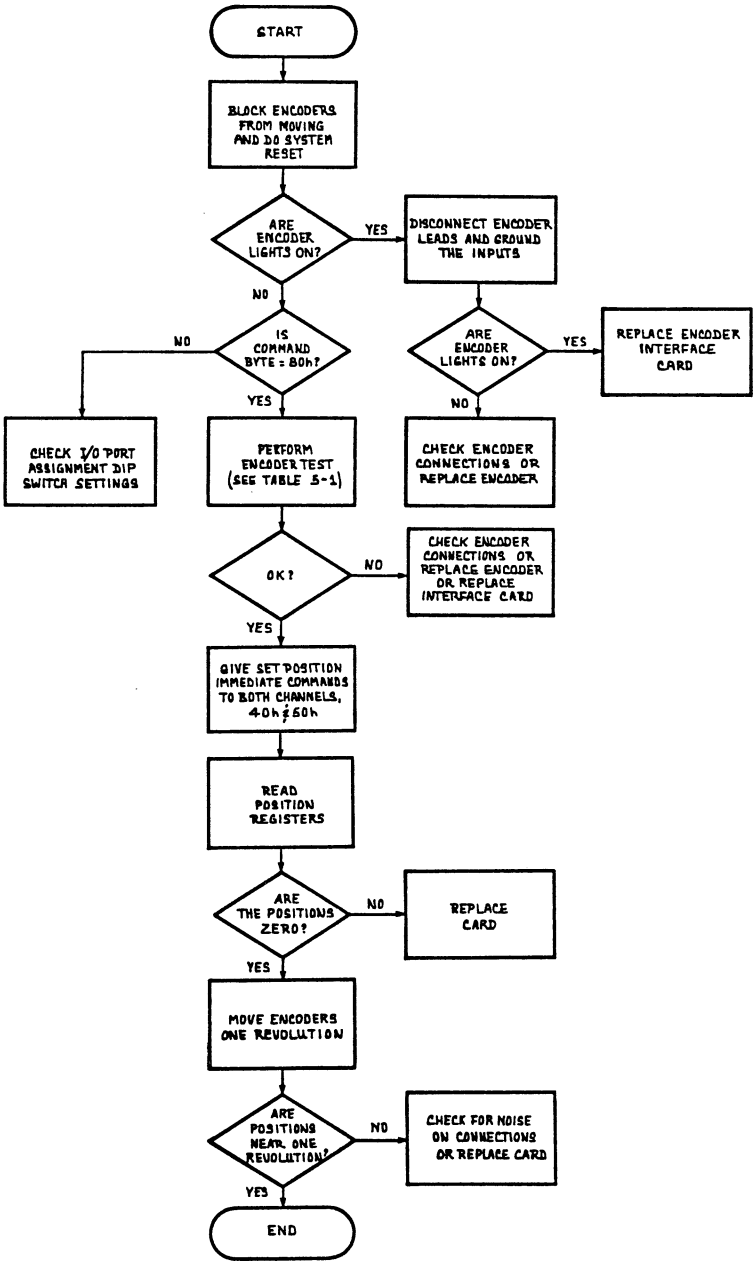


Table 5-1 Encoder Test

1. Free the encoder so you can turn it.
2. Turn the encoder in the positive direction. The green light should come on.
3. Turn the encoder in the negative direction. The yellow light should come on.

   Note: If the reverse happens, the two encoder channels are switched. See Section 2.3.

5.2 FIELD REPLACEMENT

All IBM Bus Series Incremental Encoder Interfaces are mechanically interchangeable. The cards can easily be removed from an expansion slot by removing the screw holding the card in place and pulling the card out. A new card can now be inserted. The DIP switches on the new card should be checked for correct settings for IO address mapping. Any changes in jumpers from factory shipment should be made.

APPENDIX A

SPECIFICATIONS

SPECIFICATIONS

A.1 PERFORMANCE

Position Resolution:	1X, 2X or 4X encoder resolution
Position Pulse Counting Range:	0-4,294,967,296 or +/-2,147,483,648
Maximum Pulse Frequency:	1 megahertz

A.2 MAPPING

The IBM Bus Series Incremental Encoder Interface occupies 32 consecutive I/O addresses. Port assignment is D.I.P. switch programmable to any 32 byte boundary. The cards are typically shipped from the factory at port addresses 300h through 31Fh.

A.3 ELECTRICAL

ENCODER COMPATIBILITY

Two Channel Incremental, Sine or Square Wave Output
Outputs Single-ended or Differential
Output Voltage +/-5, +/-12, +/-15 vdc
Maximum Encoder Frequency 500 kilohertz (position pulse frequency may be up to 1 megahertz)

USER INPUTS AND OUTPUTS

Outputs: 24 VDC (max.), 125 ma sink current (max.)

Inputs: 15 VDC (max.)

Connector: 26 pin ribbon cable, 0.100" center/3M part No. 3399 or equivalent for Dual Channel Interface, or 50 pin ribbon cable, 0.100" center/3M part No. 3425 or equivalent for Quad Channel Interface. Connector layout shown in Figures A-1 and A-2; pin out connections shown in Tables A-1 and A-2.

Figure A-1 User Input and Output Connector Layout
Dual Channel

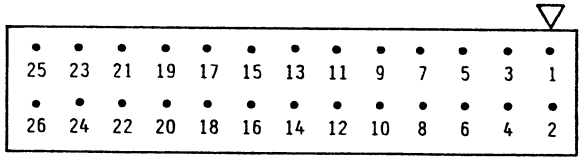


Figure A-1 User Input and Output Connector Layout
Quad Channel

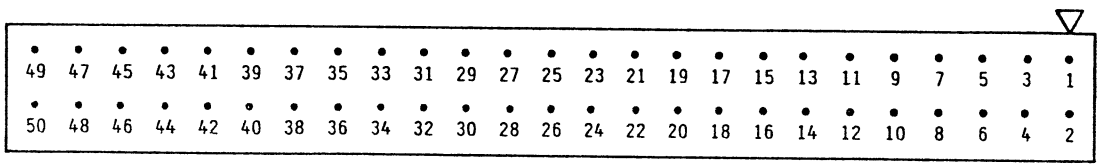


Table A-1 User Input and Output Connector Pin Outs
Dual and Quad Channel

	Pin	Mnemonic	Signal Flow	Description
Encoder Connections	25	+12 VDC	out	+12 VDC encoder supply
	24	Ground	return	Sgnl. gnd. & DC return
	26	+5 VDC	out	+5 VDC encoder supply
	1	Chnl. 1 A+	in	Encoder Chnl. 1 A+ input
	2	Chnl. 1 A-	in	Encoder Chnl. 1 A- input
	3	Chnl. 1 B+	in	Encoder Chnl. 1 B+ input
	4	Chnl. 1 B-	in	Encoder Chnl. 1 B- input
	5	Index 1 +	in	Encoder index 1 + input
	6	Index 1 -	in	Encoder index 1 - input
	13	Chnl. 2 A+	in	Encoder Chnl. 2 A+ input
	14	Chnl. 2 A-	in	Encoder Chnl. 2 A- input
	15	Chnl. 2 B+	in	Encoder Chnl. 2 B+ input
	16	Chnl. 2 B-	in	Encoder Chnl. 2 B- input
	17	Index 2 +	in	Encoder index 2 + input
	18	Index 2 -	in	Encoder index 2 - input
Outputs	8	Set Pt. 11*	out	Chnl. 1 set point 1
	9	Set Pt. 12*	out	Chnl. 1 set point 2
	10	Set Pt. 13*	out	Chnl. 1 set point 3
	11	Set Pt. 14*	out	Chnl. 1 set point 4
	20	Set Pt. 21*	out	Chnl. 2 set point 1
	21	Set Pt. 22*	out	Chnl. 2 set point 2
	22	Set Pt. 23*	out	Chnl. 2 set point 3
	23	Set Pt. 24*	out	Chnl. 2 set point 4
Inputs	7	Home 1*	in	Chnl. 1 home input
	12	Pull-up	in	Pull-up voltage input
	19	Home 2*	in	Chnl. 2 home input

Table A-2 User Input and Output Connector Pin Outs
Quad Channel

	Pin	Mnemonic	Signal Flow	Description
Encoder	50	Ground	return	Sgnl. gnd. & DC return
Connections	27	Chnl. 3 A+	in	Encoder Chnl. 3 A+ input
	28	Chnl. 3 A-	in	Encoder Chnl. 3 A- input
	29	Chnl. 3 B+	in	Encoder Chnl. 3 B+ input
	30	Chnl. 3 B-	in	Encoder Chnl. 3 B- input
	31	Index 3 +	in	Encoder index 3 + input
	32	Index 3 -	in	Encoder index 3 - input
	39	Chnl. 4 A+	in	Encoder Chnl. 4 A+ input
	40	Chnl. 4 A-	in	Encoder Chnl. 4 A- input
	41	Chnl. 4 B+	in	Encoder Chnl. 4 B+ input
	42	Chnl. 4 B-	in	Encoder Chnl. 4 B- input
	43	Index 4 +	in	Encoder index 4 + input
	44	Index 4 -	in	Encoder index 4 - input
Outputs	34	Set Pt. 31*	out	Chnl. 3 set point 1
	35	Set Pt. 32*	out	Chnl. 3 set point 2
	36	Set Pt. 33*	out	Chnl. 3 set point 3
	37	Set Pt. 34*	out	Chnl. 3 set point 4
	46	Set Pt. 41*	out	Chnl. 4 set point 1
	47	Set Pt. 42*	out	Chnl. 4 set point 2
	48	Set Pt. 43*	out	Chnl. 4 set point 3
	49	Set Pt. 44*	out	Chnl. 4 set point 4
Inputs	33	Home 3*	in	Chnl. 3 home input
	38	Pull-up	in	Pull-up voltage input
	45	Home 4*	in	Chnl. 4 home input

TIMING

Position Register Access: 50 microseconds maximum
Position Information Delay: 500 microseconds maximum,
250 microseconds typical

POWER SUPPLY REQUIREMENTS

Dual: +5VDC +/- 5% @ 1.2 Amps max., 0.9 Amps typical;
Quad: +5VDC +/- 5% @ 2.0 Amps max., 1.5 Amps typical;
encoder requirements not included

BUS INTERFACE

The Incremental Encoder Interface meets all IBM Bus General Electrical Specifications. All bus inputs are 2 LSTTL loads maximum. All bus outputs drive 55 LSTTL loads minimum. The card is compatible with systems up to 8.0 megahertz. Table A-3 below lists the IBM Bus Connector Pin Outs:

Table A-3 IBM Bus Connector Pin Outs

Pin	Mnemonic	Signal Flow	Remarks
A1	I/O CH CK*	not used	
A2	D7	in/out	(Tri-state input/output active
A3	D6		high) D0-D7 constitute an 8
A4	D5		bit bidirectional data bus
A5	D4		which is used for all data
A6	D3		exchange between the host
A7	D2		computer and the card.
A8	D1		
A9	D0		
A10	I/O CH RDY	out	I/O Channel Ready (output active high) Pulled low by the card immediately upon detecting a valid address from the host computer.
A11	AEN	in	Address Enable (input active high) When active, signifies a DMA access.
A12	A19	not used	
A13	A18	not used	
A14	A17	not used	
A15	A16	not used	
A16	A15	not used	
A17	A14	not used	
A18	A13	not used	
A19	A12	not used	
A20	A11	not used	
A21	A10	not used	
A22	A9	in	(Input only) The address bus
A23	A8	in	is used to decode the location
A24	A7	in	of the card in the 1024 port
A25	A6	in	I/O field. Only the lower 10
A26	A5	in	bits (A0-A9) are used. A0 is
A27	A4	in	the least significant bit and
A28	A3	in	A9 is the most.
A29	A2	in	
A30	A1	in	
A31	A0	in	

TABLE A-3 IBM Bus Connector Pin Outs
(cont.)

Pin	Mnemonic	Signal Flow	Remarks
B1	GND	return	Ground-System signal ground and DC return
B2	RESET DRV	not used	
B3	+5V	in	+5 VDC System Power
B4	IRQ2	out	Refer to IRQ7
B5	-5VDC	not used	
B6	DRQ2	not used	
B7	-12V	not used	
B8	RESERVED	not used	
B9	+12V	in	+12 VDC System Power
B10	GND	return	Ground-System signal ground and DC return
B11	MEMW*	not used	
B12	MEMR*	not used	
B13	IOW*	in	I/O Write (input active low) Signals the card to read data on data bus.
B14	IOR*	in	I/O Read (input active low) Signals the card to write data onto data bus.
B15	DACK3*	not used	
B16	DRQ3	not used	
B17	DACK1*	not used	
B18	DRQ1	not used	
B19	DACK0*	not used	
B20	CLOCK	not used	
B21	IRQ7	out	Interrupt Request 2 to 7
B22	IRQ6	out	(output active high) Used
B23	IRQ5	out	to signal host for service.
B24	IRQ4	out	IRQ2 is higest priority and
B25	IRQ3	out	IRQ7 is lowest.
B26	DACK2*	not used	
B27	T/C	not used	
B28	ALE*	not used	
B29	+5V	in	+5 VDC System Power
B30	OSC	not used	
B31	GND	return	Ground-System signal ground and DC return

A.4 ENVIRONMENTAL

Operating Temperature: 0 to 65 degrees C. free air ambient
Storage Temperature: -40 to 80 degrees C.

A.5 MECHANICAL

The IBM Bus Incremental Encoder Interface adheres to all IBM Bus mechanical specifications.

APPENDIX B

SUMMARY OF COMMANDS

Table B-1 Summary of Commands

COMMAND (HEX)	COMMAND (DECIMAL)	FUNCTION
00	0	COLD BOOT: executes software reset
01	1	MASTER ENABLE INT.: enables all interrupts
02	2	MASTER DISABLE INT.: disables all interrupts
03	3	CLEAR INT.: clears all pending interrupts
04	4	INT. ACK. clears highest priority interrupt
05	5	READ INT. BITS: puts int. bits in Data Reg.
06	6	ENABLE CHANNEL 1(3) INTERRUPTS
07	7	DISABLE CHANNEL 1(3) INTERRUPTS
08	8	RESET CHAN. 1(3) INT.: clears chan. 1(3) int. sources
09	9	CLEAR CHANNEL 1(3) OVERFLOW
0A	10	LOAD: loads chan. 1(3) position pulse multiplier
0B	11	LOAD: loads chan. 1(3) position range type
16	22	ENABLE CHANNEL 2(4) INTERRUPTS
17	23	DISABLE CHANNEL 2(4) INTERRUPTS
18	24	RESET CHAN. 2(4) INT.: clears chan. 2(4) int. sources
19	25	CLEAR CHANNEL 2(4) OVERFLOW
1A	26	LOAD: loads chan. 2(4) position pulse multiplier
1B	27	LOAD: loads chan. 2(4) position range type
20	32	SET POINT: point 1(3)1 enabled when greater than
21	33	SET POINT: point 1(3)1 enabled when less than
22	34	SET POINT: point 1(3)1 enabled when between
23	35	SET POINT: point 1(3)1 turned off
24	36	SET POINT: point 1(3)2 enabled when greater than
25	37	SET POINT: point 1(3)2 enabled when less than
26	38	SET POINT: point 1(3)2 enabled when between
27	39	SET POINT: point 1(3)2 turned off
28	40	SET POINT: point 1(3)3 enabled when greater than
29	41	SET POINT: point 1(3)3 enabled when less than
2A	42	SET POINT: point 1(3)3 enabled when between
2B	43	SET POINT: point 1(3)3 turned off
2C	44	SET POINT: point 1(3)4 enabled when greater than
2D	45	SET POINT: point 1(3)4 enabled when less than
2E	46	SET POINT: point 1(3)4 enabled when between
2F	47	SET POINT: point 1(3)4 turned off
30	48	SET POINT: point 2(4)1 enabled when greater than
31	49	SET POINT: point 2(4)1 enabled when less than
32	50	SET POINT: point 2(4)1 enabled when between
33	51	SET POINT: point 2(4)1 turned off
34	52	SET POINT: point 2(4)2 enabled when greater than
35	53	SET POINT: point 2(4)2 enabled when less than
36	54	SET POINT: point 2(4)2 enabled when between
37	55	SET POINT: point 2(4)2 turned off
38	56	SET POINT: point 2(4)3 enabled when greater than
39	57	SET POINT: point 2(4)3 enabled when less than
3A	58	SET POINT: point 2(4)3 enabled when between
3B	59	SET POINT: point 2(4)3 turned off
3C	60	SET POINT: point 2(4)4 enabled when greater than
3D	61	SET POINT: point 2(4)4 enabled when less than
3E	62	SET POINT: point 2(4)4 enabled when between
3F	63	SET POINT: point 2(4)4 turned off

Table B-1 Summary of Commands
(cont.)

COMMAND (HEX)	COMMAND (DECIMAL)	FUNCTION
40	64	SET: immediately set 1(3) at middle of range
41	65	SET: immediately set 1(3) position in Data Reg.
44	68	SET: find home, set 1(3) at middle of range
45	69	SET: find home, set 1(3) at position in Data Reg.
48	72	SET: find index, set 1(3) at middle of range
49	73	SET: find index, set 1(3) at position in Data Reg.
4C	76	SET: find both, set 1(3) at middle of range
4D	77	SET: find both, set 1(3) at position in Data Reg.
50	80	SET: immediately set 2(4) at middle of range
51	81	SET: immediately set 2(4) at position in Data Reg.
54	84	SET: find home, set 2(4) at middle of range
55	85	SET: find home, set 2(4) at position in Data Reg.
58	88	SET: find index, set 2(4) at middle of range
59	89	SET: find index, set 2(4) at position in Data Reg.
5C	92	SET: find both, set 2(4) at middle of range
5D	93	SET: find both, set 2(4) at position in Data Reg.
60	96	INTERRUPT: point 1(3)1 high to low transition
61	97	INTERRUPT: point 1(3)1 low to high transition
62	98	INTERRUPT: point 1(3)1 low
63	99	INTERRUPT: point 1(3)1 high
64	100	INTERRUPT: point 1(3)2 high to low transition
65	101	INTERRUPT: point 1(3)2 low to high transition
66	102	INTERRUPT: point 1(3)2 low
67	103	INTERRUPT: point 1(3)2 high
68	104	INTERRUPT: point 1(3)3 high to low transition
69	105	INTERRUPT: point 1(3)3 low to high transition
6A	106	INTERRUPT: point 1(3)3 low
6B	107	INTERRUPT: point 1(3)3 high
6C	108	INTERRUPT: point 1(3)4 high to low transition
6D	109	INTERRUPT: point 1(3)4 low to high transition
6E	110	INTERRUPT: point 1(3)4 low
6F	111	INTERRUPT: point 1(3)4 high
70	112	INTERRUPT: point 2(4)1 high to low transition
71	113	INTERRUPT: point 2(4)1 low to high transition
72	114	INTERRUPT: point 2(4)1 low
73	115	INTERRUPT: point 2(4)1 high
74	116	INTERRUPT: point 2(4)2 high to low transition
75	117	INTERRUPT: point 2(4)2 low to high transition
76	118	INTERRUPT: point 2(4)2 low
77	119	INTERRUPT: point 2(4)2 high
78	120	INTERRUPT: point 2(4)3 high to low transition
79	121	INTERRUPT: point 2(4)3 low to high transition
7A	122	INTERRUPT: point 2(4)3 low
7B	123	INTERRUPT: point 2(4)3 high
7C	124	INTERRUPT: point 2(4)4 high to low transition
7D	125	INTERRUPT: point 2(4)4 low to high transition
7E	126	INTERRUPT: point 2(4)4 low
7F	127	INTERRUPT: point 2(4)4 high

APPENDIX C

DEFAULT SETTINGS

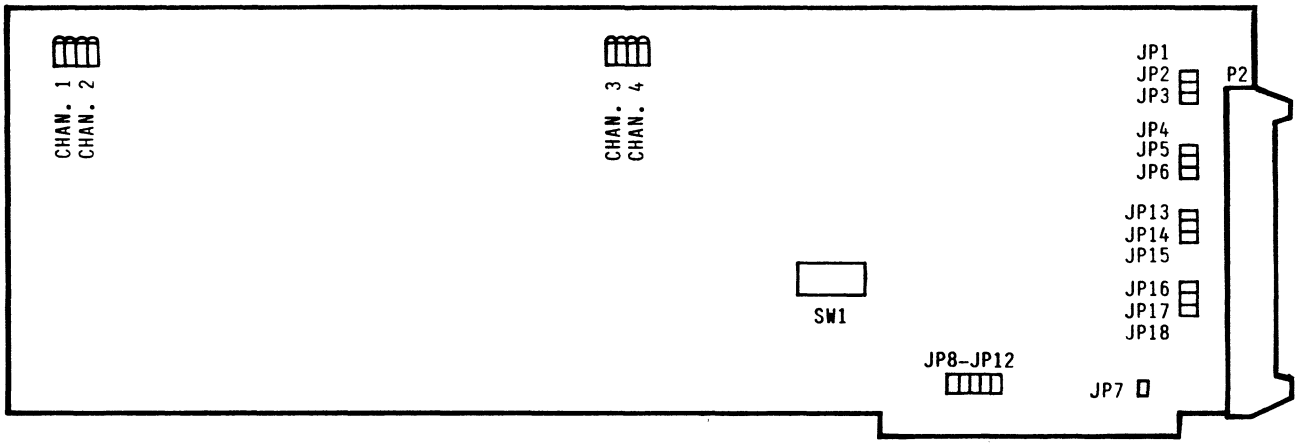
Table C-1 Default Settings

PARAMETER	SETTING
Master Interrupts	Disabled
Channel 1 Interrupts	Disabled, all interrupt sources reset
Channel 1 PPM	1
Channel 1 Range	1 (signed)
Channel 1 Position	0
Channel 1 Set Points	off
Channel 2 Interrupts	Disabled, all interrupt sources reset
Channel 2 PPM	1
Channel 2 Range	1 (signed)
Channel 2 Position	0
Channel 2 Set Points	off
Channel 3 Interrupts	Disabled, all interrupt sources reset
Channel 3 PPM	1
Channel 3 Range	1 (signed)
Channel 3 Position	0
Channel 3 Set Points	off
Channel 4 Interrupts	Disabled, all interrupt sources reset
Channel 4 PPM	1
Channel 4 Range	1 (signed)
Channel 4 Position	0
Channel 4 Set Points	off

APPENDIX D

MODULE CONFIGURATION

Figure Module Configuration Worksheet
Incremental Encoder Interface



SETTINGS	
SW1	CARD MAPPED TO:
JP1,2,3	CHANNEL 1 CONFIGURED FOR: ☐ SINGLE-ENDED ENCODERS ☐ DIFFERENTIAL ENCODERS
JP4,5,6	CHANNEL 2 CONFIGURED FOR: ☐ SINGLE-ENDED ENCODERS ☐ DIFFERENTIAL ENCODERS
JP13,14,15	CHANNEL 3 CONFIGURED FOR: ☐ SINGLE-ENDED ENCODERS ☐ DIFFERENTIAL ENCODERS
JP16,17,18	CHANNEL 4 CONFIGURED FOR: ☐ SINGLE-ENDED ENCODERS ☐ DIFFERENTIAL ENCODERS
JP7-12	CARD CONFIGURED FOR INTERRUPTS ON IRQ__