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VME Series Incremental Encoder Interface

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GE Fanuc Automation

Programmable Control Products

VME Series
Incremental Encoder Interface

User's Manual

GFK-2199 *July 2002*

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Content of this Manual

This manual applies to the Incremental Encoder Interface model VME-3570-0.

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Additional information about Motion solutions is available at
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SECTION 1.0

GENERAL DESCRIPTION

1.1 INTRODUCTION

The Whedco VME Series Dual Channel Incremental Encoder Interface makes position feedback with an incremental encoder simple and reliable. The interface accepts quadrature and index pulse input signals from one or two encoders. Four parallel outputs per channel are available for set point triggers. In addition, the starting reference position may be initialized to any given value within the counting range. Home position may also be specified at the user's discretion as the occurrence of the index pulse, a home limit switch input, or as the occurrence of the two in tandem.

The interface is completely self-contained and supervises the entire counting and conversion routine after receiving command instructions from the host CPU. Position data is stored on-board until requested by the host.

1.2 FEATURES

Complete signal conversion and conditioning for one or two independent channels of incremental encoder interface.

Resident microprocessor and proprietary firmware supervise counting and conversion routines, thus minimizing time requirements on the host CPU.

Accommodates single-ended or differential inputs up to +/- 15 VDC.

Tracks accumulated position to 4,294,967,296 pulses or +/- 2,147,483,648.

Four set points per channel can be programmed as active when the position counters are less than or greater than the set point position or within a range between two positions.

Position pulse multiplier provides for position resolution one, two, or four times greater than encoder line density.

SECTION 2.0

INSTALLATION

2.1 INSPECTION

Before installing or applying power to the card, visually inspect it and assert that there is no shipping damage. If, by chance, any I.C. has been shaken out of its socket in transit, reinsert the loose leads into the socket.

2.2 MAPPING

The encoder interface occupies 256 consecutive I/O addresses. Port assignment is D.I.P. switch programmable to any 256 byte boundary (page) in the 65,536 byte short address space. The card is shipped from the factory at port addresses 0h through FFh (page 0). The I/O ports can be changed using D.I.P switch SW1 located near the 96 pin DIN connector. The desired page is selected by programming SW1 with the binary equivalent of the page number where a one corresponds to an open position and a zero corresponds to a closed position. Position 1 is the least significant digit and position 8 is the most significant digit.

2.3 INCREMENTAL ENCODER CONNECTIONS

The encoder interface provides input lines for single-ended or differential output encoders as well as a power output line for 5 or 12 volt encoders. 15 volt encoders will require an external power supply. The index line can be optionally connected provided the encoder is so equipped.

To connect the encoders, simply follow the diagrams given in Figures 2-1, 2-2, 2-3, and 2-4. Keep in mind that shorting plugs must be installed in jumpers JP1, JP2, and JP3 for channel one and jumpers JP4, JP5, and JP6 for channel two when using single-ended encoders and removed when using differential. Refer to Appendix E for the location of the jumpers. The card comes shipped with the shorting plugs installed. Note that JP7 must be jumpered properly for operation with 5 or 12 volt encoders. The shorting plug should placed on the two pins closest to the LEDs for 5 volt encoders and on the two pins furtherest away from the LEDs for 12 volt encoders. The card is shipped jumpered for 5 volt encoders.

The encoder interface comes with two LEDs per channel which indicate the direction in which the encoder is turning. When turning in the positive direction, the corresponding green LED lights. When turning in the negative direction, the corresponding yellow LED lights. These LEDs are helpful in determining that the encoders are working properly and that the polarity of the encoder connections are correct.

Figure 2-1 Interfacing to a Single-Ended Encoder without an External Power Supply

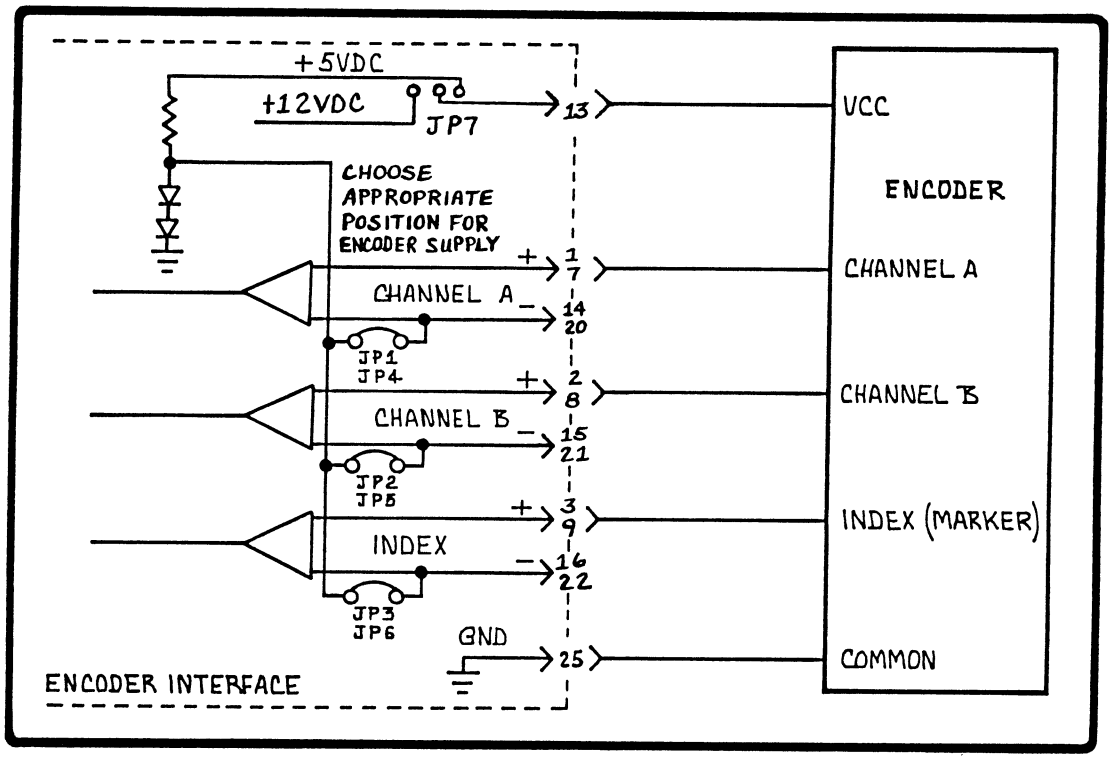


Figure 2-2 Interfacing to a Single Ended Encoder with an External Power Supply

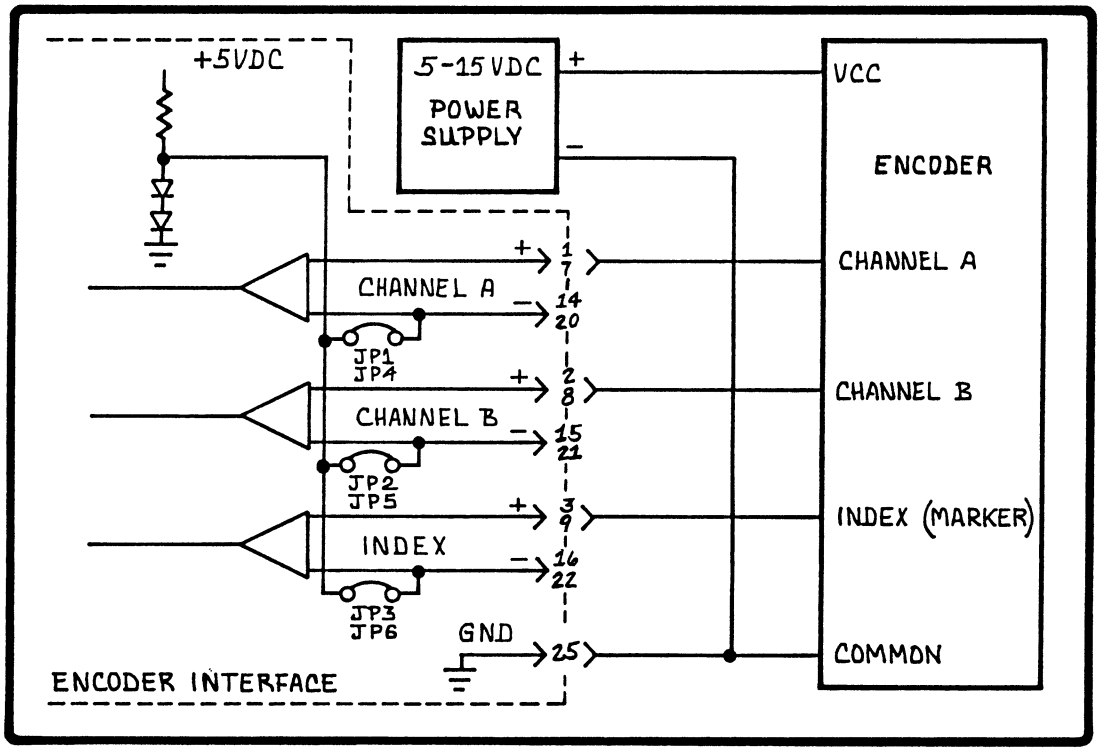


Figure 2-3 Interfacing to a Differential Encoder without an External Power Supply

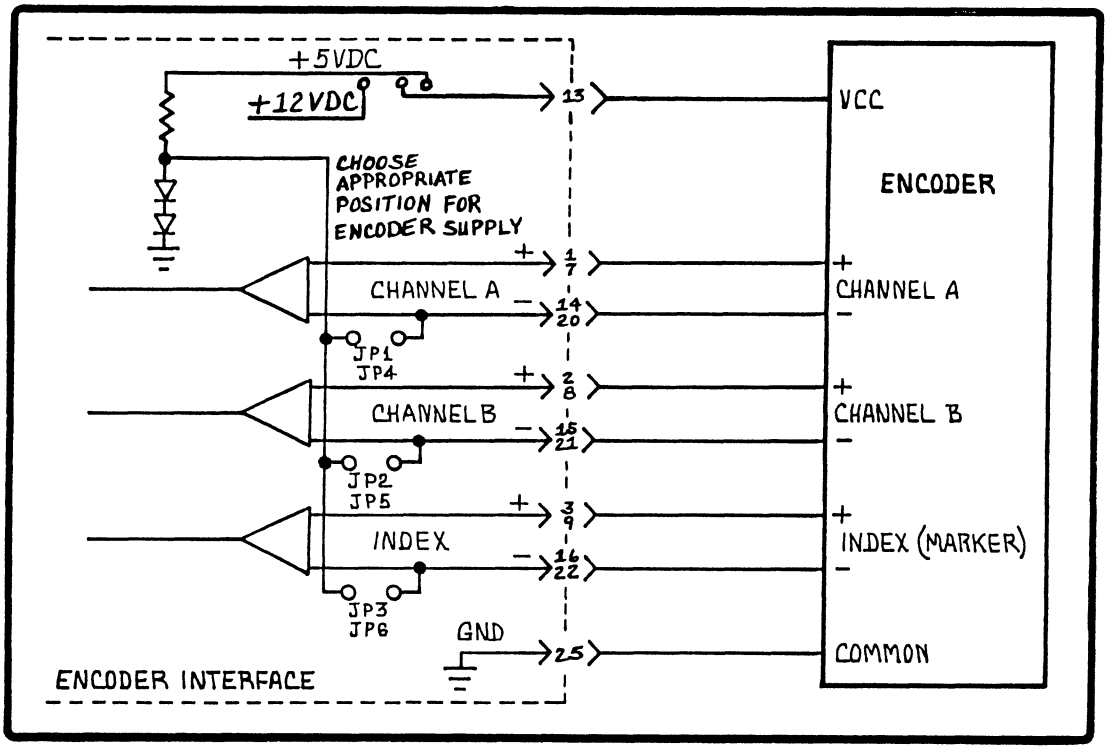
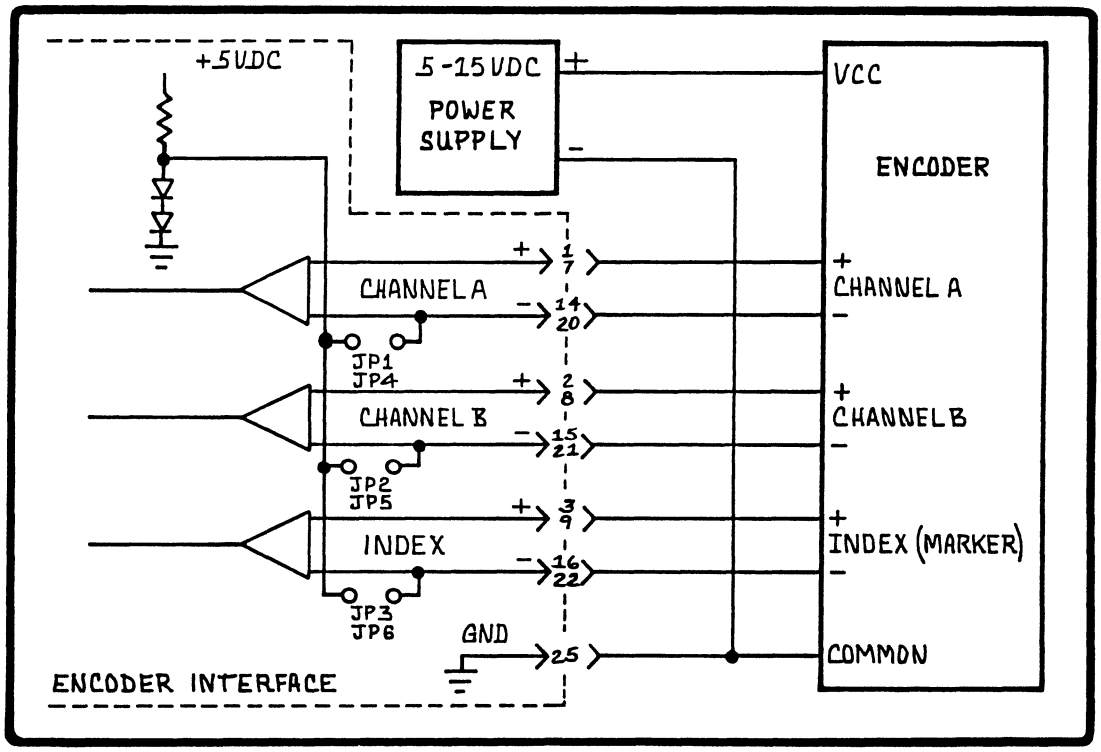


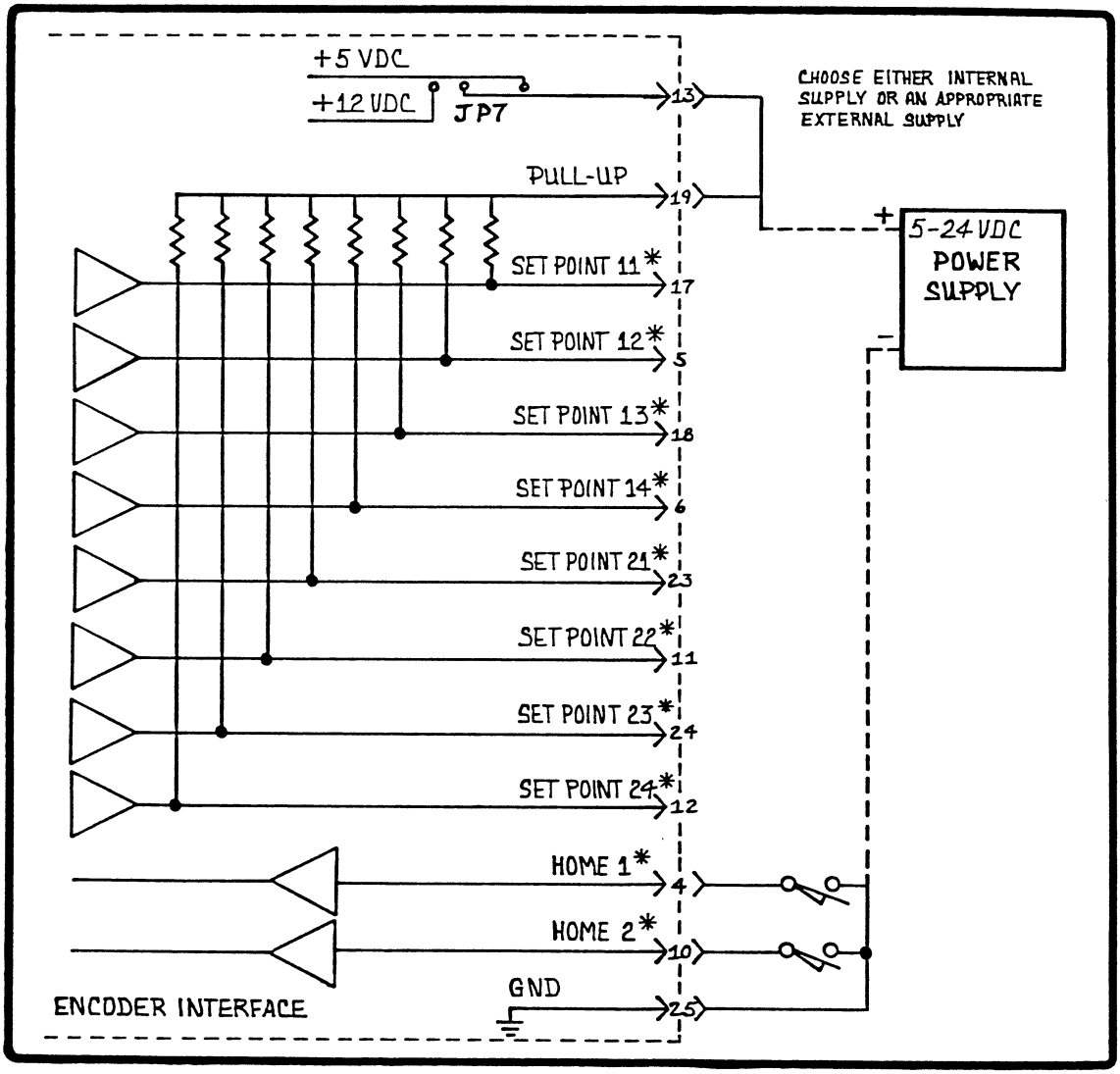
Figure 2-4 Interfacing to a Differential Encoder with an External Power Supply



2.4 I/O LINES

The encoder interface provides a home input line and 4 set point output lines per encoder. For a pin out of the I/O connector, see Appendix A, Section A.3. The home input lines are active low and can accept voltages up to 15 vdc. The output lines are active low also. They are sinking outputs and will sink up to 125mA at up to 24 volts. The Pull-Up line should be connected to the interface voltage used. The encoder power supply line can be used if appropriate. For a connection diagram, see Figure 2-5.

Figure 2-5 Typical Connection of I/O Lines



"*" = Signal is active low.

SECTION 3.0

OPERATION

3.1 READING FROM AND WRITING TO THE I/O REGISTERS

The encoder interface has 16 registers through which it communicates with the host CPU. Eight registers hold the two 32 bit position counters. Four registers transfer data back and forth. One provides the position handshake. One holds the status of the set points. One contains the status of the encoder interface, and one is used to give the interface commands. The assignment of the I/O registers to the port locations is given in Table 3-1.

Table 3-1 I/O Register Assignment

XX01	low	
XX03		Channel 1 Position
XX05		
XX07	high	
XX09	low	
XX0B		Channel 2 position
XX0D		
XX0F	high	
XX11	low	
XX13		Data
XX15		
XX17	high	
XX19		Position Handshake
XX1B		Set Points
XX1D		Status
XX1F		Command

"XX" = base address (see Section 2.2)

The encoder interface responds to the Short Supervisory Access and Short Non-Privileged Access Address Modifier Codes only. It is capable of single odd byte transfers only. It will not respond to any other type of transfer.

Any of the 16 I/O registers may be written to or read by the host CPU at any time except for the Command Register which should only be written to when the most significant bit (bit 7) is set. This is the Ready for Command Bit. The encoder interface causes the host to wait in response to a write or read to the I/O registers until the current on-board bus cycle is completed. This means a typical wait of 0.2 - 1.4 microseconds.

The host access disables the interface CPU (puts the Z-80 into the DMA mode) during the host read or write. This causes no problem as long as the accesses are not more than 25% of the interface CPU's time or a regular basis of not more than one every 32 microseconds. Therefore, exercise caution when writing tight loops which wait for one of the flags to change state. If the system CPU accesses too often, the interface CPU may not be able to keep up with the incoming encoder pulses and lose some of them.

3.2 OPERATING STATUS

The encoder interface has a Status Register which provides information on the operation of the card. Table 3-2 lists the bits in the register and the purpose of each.

Table 3-2 Status Register Bits

BIT	LABEL	DESCRIPTION
B0	CHNL. 1 HOME	This bit reflects the status of channel 1 home input. 1 = input low (active)
B1	CHNL. 1 INDEX	This bit reflects the status of channel 1 index pulse. 1 = input high (active)
B2	CHNL. 1 OVERFLOW	If channel 1 Position Register over- or underflows, this bit becomes true. It can be reset by using the Clear Channel 1 Overflow Command (09h).
B3	CHNL. 2 HOME	This bit reflects the status of channel 2 home input. 1 = input low (active)
B4	CHNL. 2 INDEX	This bit reflects the status of channel 2 index pulse. 1 = input high (active)
B5	CHNL. 2 OVERFLOW	If channel 2 Position Register over- or underflows, this bit becomes true. It can be reset by using the Clear Channel 2 Overflow Command (19h).
B6	none	No function
B7	POSITION AVAILABLE	When this bit is true, the card is not updating the Position Registers which makes the registers available to be read.

Note: If bit = 1, then condition is true

3.3 READING POSITION

To avoid the possibility of getting contaminated data, a particular handshake procedure should be used when reading the Position Registers. This procedure is as follows:

1) Set the Request Position Bit (bit 0) of the Position Handshake Register to one.
2) Wait for the Position Available Bit (bit 7) of the Status Register to be one.
3) Read the Position Registers.
4) Reset the Request Position Bit to zero.

It is important to always perform the last step since the encoder interface will not update the Position Registers when the Request Position Bit is true.

SECTION 4.0

PROGRAMMING

4.1 INTRODUCTION

To program the VME Series Dual Channel Incremental Encoder Interface, the host CPU writes commands to the command port. This is done by first waiting for the most significant bit (bit 7) of the command port to be true. This is the Ready for Command Bit. After this bit is high, the data port should be loaded with any pertinent information needed for the command and then the particular command should be written to the command port.

After the encoder interface has been programmed, the host CPU can periodically read the status and set point ports to check up on the encoders. In addition, at any time, the host CPU can read the 32 bit position counters for each channel by making use of the position handshake procedure discussed in Section 3.3.

4.2 PARAMETERS

Two parameters define operation of the counters which need to be loaded after power up or after a software reset command. The first, Position Pulse Multiplier, determines how many pulses should be counted for each line on the encoder. Its valid values are "1" for one count per line (default), "2" for two counts per line, or "4" for four counts per line. The command to load it is 10 (0Ah) for Channel One and 26 (1Ah) for Channel Two.

The second parameter is Position Range Type. When this parameter is 0, the range of the counter is from 0 to 4,294,967,296. When the parameter is 1 (default), the range of the counter is from -2,147,483,648 to 2,147,483,647 in 2's complement notation. The command to load it is 11 (0Bh) for Channel One and 27 (1Bh) for Channel Two.

4.3 SETTING POSITION

Upon power up or after a software reset, the position counters are set to the middle of their ranges which are 2,147,483,648 for the unsigned range and 0 for the signed range. To change the position, at any time, the Set Position Command is used. This command has several modifiers associated with it to select which channel's counter to set, when to perform the set, and to what value the counter should be set. See Table 4-1 for a listing of the command byte needed for each type of position set.

Table 4-1 Command Byte for Specified Position Sets

TYPE OF POSITION SET	COMMAND (HEX)	(DECIMAL)
Channel 1:		
Immediately set at middle of range	40	64
Immediately set at position in Data Register	41	65
Find home, set at middle of range	44	68
Find home, set at position in Data Register	45	69
Find index, set at middle of range	48	72
Find index, set at position in Data Register	49	73
Find home & index, set at middle of range	4C	76
Find home & index, set at Data Register	4D	77
Channel 2:		
Immediately set at middle of range	50	80
Immediately set at position in Data Register	51	81
Find home, set at middle of range	54	84
Find home, set at position in Data Register	55	85
Find index, set at middle of range	58	88
Find index, set at position in Data Register	59	89
Find home & index, set at middle of range	5C	92
Find home & index, set at Data Register	5D	93

4.4 SET POINTS

Each channel has four set points which can be set to any location over the entire range of the position counters. Each has a flag and an output line with which it is associated. The flags are located in the Set Point Register. Channel 1, point 1, is assigned to bit 0; channel 1, point 2, to bit 1, and so forth. Channel 2 begins with bit 4. The output lines are listed in Appendix A, Table A-1.

These set points can be programmed to be active when the position counters are less than the set point position, when the position counters are greater than the set point position, or when the position counters are between the two set point positions. The set points are programmed by first loading the Data Register with the set point location and then issuing the appropriate version of the Set Point Command. To program a set point to be active between two positions, the lower position is loaded first by the above method. Then the higher position is loaded with the above method using the same Set Point Command as before. Table 4-2 lists the command for different cases.

Table 4-2 Command Byte for Specific Set Point Cases

SET POINT CASE	COMMAND (HEX)	(DECIMAL)
Channel 1:		
Set point 1 enabled when greater than	20	32
Set point 1 enabled when less than	21	33
Set point 1 enabled when between	22	34
Set point 1 turned off	23	35
Set point 2 enabled when greater than	24	36
Set point 2 enabled when less than	25	37
Set point 2 enabled when between	26	38
Set point 2 turned off	27	39
Set point 3 enabled when greater than	28	40
Set point 3 enabled when less than	29	41
Set point 3 enabled when between	2A	42
Set point 3 turned off	2B	43
Set point 4 enabled when greater than	2C	44
Set point 4 enabled when less than	2D	45
Set point 4 enabled when between	2E	46
Set point 4 turned off	2F	47
Channel 2:		
Set point 1 enabled when greater than	30	48
Set point 1 enabled when less than	31	49
Set point 1 enabled when between	32	50
Set point 1 turned off	33	51
Set point 2 enabled when greater than	34	52
Set point 2 enabled when less than	35	53
Set point 2 enabled when between	36	54
Set point 2 turned off	37	55
Set point 3 enabled when greater than	38	56
Set point 3 enabled when less than	39	57
Set point 3 enabled when between	3A	58
Set point 3 turned off	3B	59
Set point 4 enabled when greater than	3C	60
Set point 4 enabled when less than	3D	61
Set point 4 enabled when between	3E	62
Set point 4 turned off	3F	63

4.5 PROGRAMMING EXAMPLE

An example of programming the card is provided in this section. It is coded in a pseudo code similar to BASIC.

This example shows how to set up and poll a set point using Channel 1. The channel uses the 4 times position pulse multiplier and the unsigned counter range. The set point is placed at 2,147,484,648 and is active when the counter is greater than 2,147,484,648. The flow chart to implement this is given in Figure 4-1, and a program listing is given in Table 4-3.

Figure 4-1 Programming Example

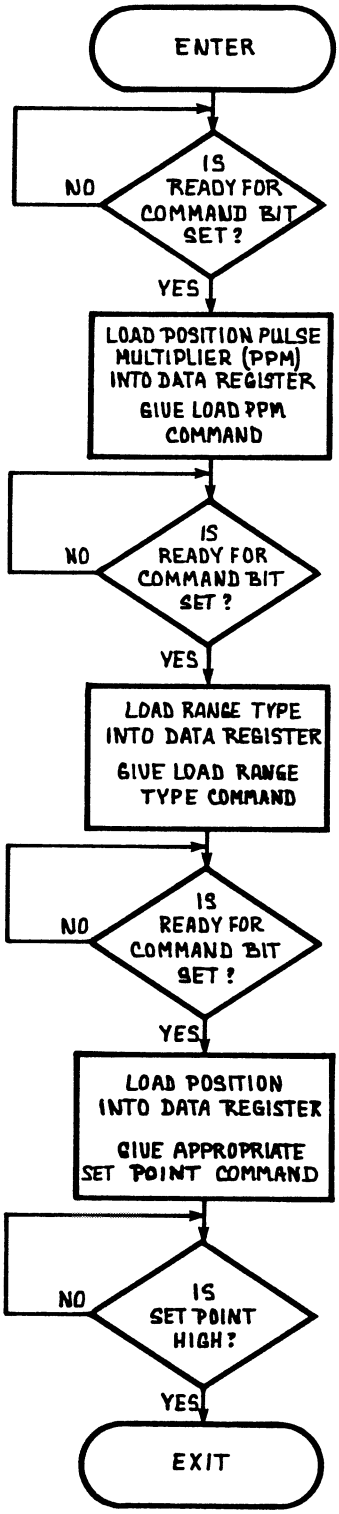


Table 4-3 Programming Example

```
; This program assumes the card is mapped at ports 00h - FFh.

START: IF NOT ( IN(1FH) AND 80H ) GOTO START ; Wait for Ready for Command
                                             ; (RFC) Bit
       OUT(11H,04H)                  ; Load position pulse multiplier (PPM)
       OUT(1FH,0AH)                  ; Give load PPM Command
LOOP1: IF NOT ( IN(1FH) AND 80H ) GOTO LOOP1 ; Wait for RFC Bit
       OUT(11H,00H)                  ; Load range type into Data Register
       OUT(1FH,0BH)                  ; Give Load Range Type Command
LOOP2: IF NOT ( IN(1FH) AND 80H ) GOTO LOOP2 ; Wait for RFC Bit
       OUT(11H,POS1)                 ; Load position into Data Register
       OUT(13H,POS1/100H)
       OUT(15H,POS1/10000H)
       OUT(17H,POS1/1000000H)
       OUT(1FH,20H)                  ; Give appropriate Set Point Command
LOOP3: IF NOT ( IN(1BH) AND 01H ) GOTO LOOP3 ; Wait for set point
```

SECTION 5.0

MAINTENANCE

5.1 TROUBLESHOOTING

If you have trouble with the card, the following flow chart and table should help you out.

Figure 5-1 Troubleshooting Flow Chart

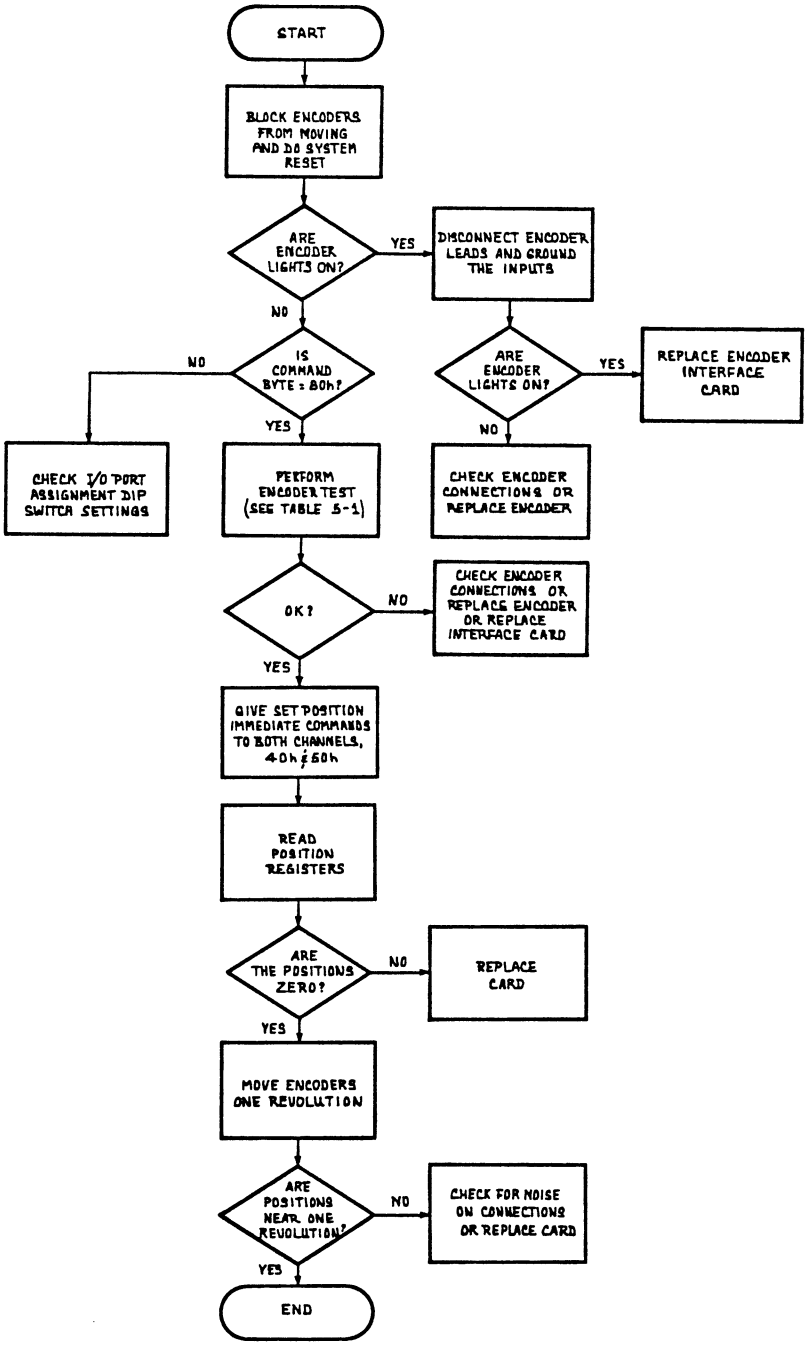


Table 5-1 Encoder Test

1. Free the encoder so you can turn it.
2. Turn the encoder in the positive direction. The green light should come on.
3. Turn the encoder in the negative direction. The yellow light should come on.

   Note: If the reverse happens, the two encoder channels are switched. See Section 2.3.

5.2 FIELD REPLACEMENT

All VME Bus Series Incremental Encoder Interfaces are mechanically interchangeable. The cards can easily be removed from an expansion slot by removing the screw holding the card in place and pulling the card out. A new card can now be inserted. The DIP switches on the new card should be checked for correct settings for IO address mapping. Any changes in jumpers from factory shipment should be made.

APPENDIX A

SPECIFICATIONS

SPECIFICATIONS

A.1 PERFORMANCE

Position Resolution:	1X, 2X or 4X encoder resolution
Position Pulse Counting Range:	0-4,294,967,296 or +/-2,147,483,648
Maximum Pulse Frequency:	500 KHz

A.2 MAPPING

The encoder interface occupies 16 consecutive I/O addresses. Port assignment is D.I.P. switch programmable to any 256 byte boundary. The cards are typically shipped from the factory at port addresses 00h through FFh.

A.3 ELECTRICAL

ENCODER COMPATIBILITY

Two Channel Incremental, Sine or Square Wave Output
Outputs Single-ended or Differential
Output Voltage +/-5, +/-12, +/-15 vdc
Maximum Encoder Frequency 500 kilohertz (position pulse frequency may be up to 1 megahertz)

USER INPUTS AND OUTPUTS

Outputs: 24 VDC (max.), 125 ma sink current (max.)

Inputs: 15 VDC (max.)

Connector: 25 pin ribbon cable, 0.100" centers/AMP part No. 747321-2 or equivalent. Connector layout shown in Figure A-1; pin out connections shown in Table A-1.

Figure A-1 User Input and Output Connector Layout

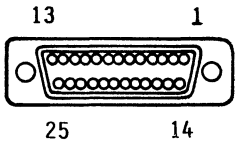


Table A-1 User Input and Output Connector Pin Outs

	Pin	Mnemonic	Signal Flow	Description
Encoder Connections	1	Chnl. 1 A+	in	Encoder Chnl. 1 A+ input
	14	Chnl. 1 A-	in	Encoder Chnl. 1 A- input
	2	Chnl. 1 B+	in	Encoder Chnl. 1 B+ input
	15	Chnl. 1 B-	in	Encoder Chnl. 1 B- input
	3	Index 1 +	in	Encoder index 1 + input
	16	Index 1 -	in	Encoder index 1 - input
	7	Chnl. 2 A+	in	Encoder Chnl. 2 A+ input
	20	Chnl. 2 A-	in	Encoder Chnl. 2 A- input
	8	Chnl. 2 B+	in	Encoder Chnl. 2 B+ input
	21	Chnl. 2 B-	in	Encoder Chnl. 2 B- input
	9	Index 2 +	in	Encoder index 2 + input
	22	Index 2 -	in	Encoder index 2 - input
	13	Encoder Power	out	Encoder power supply
	25	Ground	return	Sgnl. gnd. & DC return
Outputs	17	Set Pt. 11*	out	Chnl. 1 set point 1
	5	Set Pt. 12*	out	Chnl. 1 set point 2
	18	Set Pt. 13*	out	Chnl. 1 set point 3
	6	Set Pt. 14*	out	Chnl. 1 set point 4
	23	Set Pt. 21*	out	Chnl. 2 set point 1
	11	Set Pt. 22*	out	Chnl. 2 set point 2
	24	Set Pt. 23*	out	Chnl. 2 set point 3
	12	Set Pt. 24*	out	Chnl. 2 set point 4
Inputs	4	Home 1*	in	Chnl. 1 home input
	19	Pull-up	in	Pull-up voltage input
	10	Home 2*	in	Chnl. 2 home input

TIMING

Position Register Access: 50 microseconds maximum
Position Information Delay: 500 microseconds maximum,
250 microseconds typical

POWER SUPPLY REQUIREMENTS

+5 VDC +/- 5% @ 1.2 Amps max., 0.9 Amps typical;
encoder requirements not included

BUS INTERFACE

The Dual Channel Incremental Encoder Interface meets all VME Bus Electrical Specifications. Table A-2 below lists the VME Bus J1/P1 Connector Pin Outs:

Table A-2 VME Bus J1/P1 Connector Pin Outs

	Pin	Row	Mnemonic	Signal Flow	Remarks
System	32	a	+5V	not used	+5 VDC System Power
Power	32	b	+5V	in	+5 VDC System Power
Bus	32	c	+5V	not used	+5 VDC System Power
	9	a	GND	not used	Sgnl. gnd. & DC return
	11	a	GND	not used	Sgnl. gnd. & DC return
	15	a	GND	not used	Sgnl. gnd. & DC return
	17	a	GND	not used	Sgnl. gnd. & DC return
	19	a	GND	return	Sgnl. gnd. & DC return
	20	b	GND	not used	Sgnl. gnd. & DC return
	23	b	GND	return	Sgnl. gnd. & DC return
	9	c	GND	not used	Sgnl. gnd. & DC return
	31	a	-12V	not used	-12 VDC System Power
	31	b	+5V STDBY	not used	+5V Standby Power
	31	c	+12V	in	+12 VDC System Power
Data	1	a	D0	in/out	(Tri-State input/output active
Bus	2	a	D1	in/out	high) D0-D7 constitute an 8
	3	a	D2	in/out	bit bidirectional data bus
	4	a	D3	in/out	which is used for all data
	5	a	D4	in/out	exchange between the host
	6	a	D5	in/out	computer and the VME-3570.
	7	a	D6	in/out	
	8	a	D7	in/out	
	1	c	D8	not used	
	2	c	D9	not used	
	3	c	D10	not used	
	4	c	D11	not used	
	5	c	D12	not used	
	6	c	D13	not used	
	7	c	D14	not used	
	8	c	D15	not used	
Address	16	b	AM0	in	(Input only) The address
Modifier	17	b	AM1	in	modifier is used to determine
	18	b	AM2	in	the type of address supplied
	19	b	AM3	in	on the address bus.
	23	a	AM4	in	
	14	c	AM5	in	

Table A-2 VME Bus J1/P1 Connector Pin Outs
(cont.)

	Pin	Row	Mnemonic	Signal Flow	Remarks
Address Bus	30	a	A1	in	(Input only) The address bus is used to decode the location of the VME-3570 in the 65,536 byte short address space. Only the lower 15 bits (A1-A15) are used. A0 is the least significant bit and A15 is the most.
	29	a	A2	in	
	28	a	A3	in	
	27	a	A4	in	
	26	a	A5	not used	
	25	a	A6	not used	
	24	a	A7	not used	
	30	c	A8	in	
	29	c	A9	in	
	28	c	A10	in	
	27	c	A11	in	
	26	c	A12	in	
	25	c	A13	in	
	24	c	A14	in	
	23	c	A15	in	
	22	c	A16	not used	
	21	c	A17	not used	
	20	c	A18	not used	
	19	c	A19	not used	
	18	c	A20	not used	
	17	c	A21	not used	
	16	c	A22	not used	
	15	c	A23	not used	
Control Bus	10	a	SYSCLK	not used	System Clock
	12	a	DS1*	in	Data Strobe One (acitve low)
	13	a	DS0*	in	Data Strobe Zero (active low)
	14	a	WRITE*	in	Write (active low)
	16	a	DTACK*	out	Data Acknowledge (active low)
	18	a	AS*	not used	Address Strobe (active low)
	20	a	IACK*	in	Interrupt Acknowledge (active low)
	21	a	IACKIN*	in	Tied to IACKOUT*
	22	a	IACKOUT*	out	Tied to IACKIN*
	1	b	BBSY*	not used	Bus Busy (active low)
	2	b	BCLR*	not used	Bus Clear (active low)
	3	b	ACFAIL*	in	AC Power Fail (active low)
	4	b	BG0IN*	in	Tied to BG0OUT*
	5	b	BG0OUT*	out	Tied to BG0IN*
	6	b	BG1IN*	in	Tied to BG1OUT*
	7	b	BG1OUT*	out	Tied to BG1IN*
	8	b	BG2IN*	in	Tied to BG2OUT*
	9	b	BG2OUT*	out	Tied to BG2IN*
	10	b	BG3IN*	in	Tied to BG3OUT*
	11	b	BG3OUT*	out	Tied to BG3IN*

Table A-2 VME Bus J1/P1 Connector Pin Outs
(cont.)

Pin	Row	Mnemonic	Signal Flow	Remarks
12	b	BR0*	not used	Bus Request 0 (active low)
13	b	BR1*	not used	Bus Request 1 (active low)
14	b	BR2*	not used	Bus Request 2 (active low)
15	b	BR3*	not used	Bus Request 3 (active low)
21	b	SERCLK	not used	Serial Clock
22	b	SERDAT*	not used	Serial Data (active low)
24	b	IRQ7*	not used	Interrupt Request 7(active low)
25	b	IRQ6*	not used	Interrupt Request 6(active low)
26	b	IRQ5*	not used	Interrupt Request 5(active low)
27	b	IRQ4*	not used	Interrupt Request 4(active low)
28	b	IRQ3*	not used	Interrupt Request 3(active low)
29	b	IRQ2*	not used	Interrupt Request 2(active low)
30	b	IRQ1*	not used	Interrupt Request 1(active low)
10	c	SYSFAIL*	not used	System Fail line (active low)
11	c	BERR*	not used	Bus Error (active low)
12	c	SYSRESET*	in	System Reset (active low) Initializes the VME-3570 during power up and whenever a System Reset occurs.
13	c	LWORD*	in	Long Word (active low)

A.4 ENVIRONMENTAL

Operating Temperature: 0 to 65 degrees C. free air ambient
Storage Temperature: -40 to 80 degrees C.

A.5 MECHANICAL

The VME Bus Dual Channel Incremental Encoder Interface adheres to all VME Bus mechanical specifications for a single height board.

APPENDIX B

SUMMARY OF COMMANDS

Table B-1 Summary of Commands

COMMAND (HEX)	COMMAND (DECIMAL)	FUNCTION
00	0	COLD BOOT: executes software reset
09	9	CLEAR CHANNEL 1 OVERFLOW
0A	10	LOAD: loads chan. 1 position pulse multiplier
0B	11	LOAD: loads chan. 1 position range type
19	25	CLEAR CHANNEL 2 OVERFLOW
1A	26	LOAD: loads chan. 2 position pulse multiplier
1B	27	LOAD: loads chan. 2 position range type
20	32	SET POINT: point 11 enabled when greater than
21	33	SET POINT: point 11 enabled when less than
22	34	SET POINT: point 11 enabled when between
23	35	SET POINT: point 11 turned off
24	36	SET POINT: point 12 enabled when greater than
25	37	SET POINT: point 12 enabled when less than
26	38	SET POINT: point 12 enabled when between
27	39	SET POINT: point 12 turned off
28	40	SET POINT: point 13 enabled when greater than
29	41	SET POINT: point 13 enabled when less than
2A	42	SET POINT: point 13 enabled when between
2B	43	SET POINT: point 13 turned off
2C	44	SET POINT: point 14 enabled when greater than
2D	45	SET POINT: point 14 enabled when less than
2E	46	SET POINT: point 14 enabled when between
2F	47	SET POINT: point 14 turned off
30	48	SET POINT: point 21 enabled when greater than
31	49	SET POINT: point 21 enabled when less than
32	50	SET POINT: point 21 enabled when between
33	51	SET POINT: point 21 turned off
34	52	SET POINT: point 22 enabled when greater than
35	53	SET POINT: point 22 enabled when less than
36	54	SET POINT: point 22 enabled when between
37	55	SET POINT: point 22 turned off
38	56	SET POINT: point 23 enabled when greater than
39	57	SET POINT: point 23 enabled when less than
3A	58	SET POINT: point 23 enabled when between
3B	59	SET POINT: point 23 turned off
3C	60	SET POINT: point 24 enabled when greater than
3D	61	SET POINT: point 24 enabled when less than
3E	62	SET POINT: point 24 enabled when between
3F	63	SET POINT: point 24 turned off

Table B-1 Summary of Commands
(cont.)

COMMAND (HEX)	COMMAND (DECIMAL)	FUNCTION
40	64	SET: immediately set 1 at middle of range
41	65	SET: immediately set 1 position in Data Reg.
44	68	SET: find home, set 1 at middle of range
45	69	SET: find home, set 1 at position in Data Reg.
48	72	SET: find index, set 1 at middle of range
49	73	SET: find index, set 1 at position in Data Reg.
4C	76	SET: find both, set 1 at middle of range
4D	77	SET: find both, set 1 at position in Data Reg.
50	80	SET: immediately set 2 at middle of range
51	81	SET: immediately set 2 at position in Data Reg.
54	84	SET: find home, set 2 at middle of range
55	85	SET: find home, set 2 at position in Data Reg.
58	88	SET: find index, set 2 at middle of range
59	89	SET: find index, set 2 at position in Data Reg.
5C	92	SET: find both, set 2 at middle of range
5D	93	SET: find both, set 2 at position in Data Reg.

APPENDIX C

DEFAULT SETTINGS

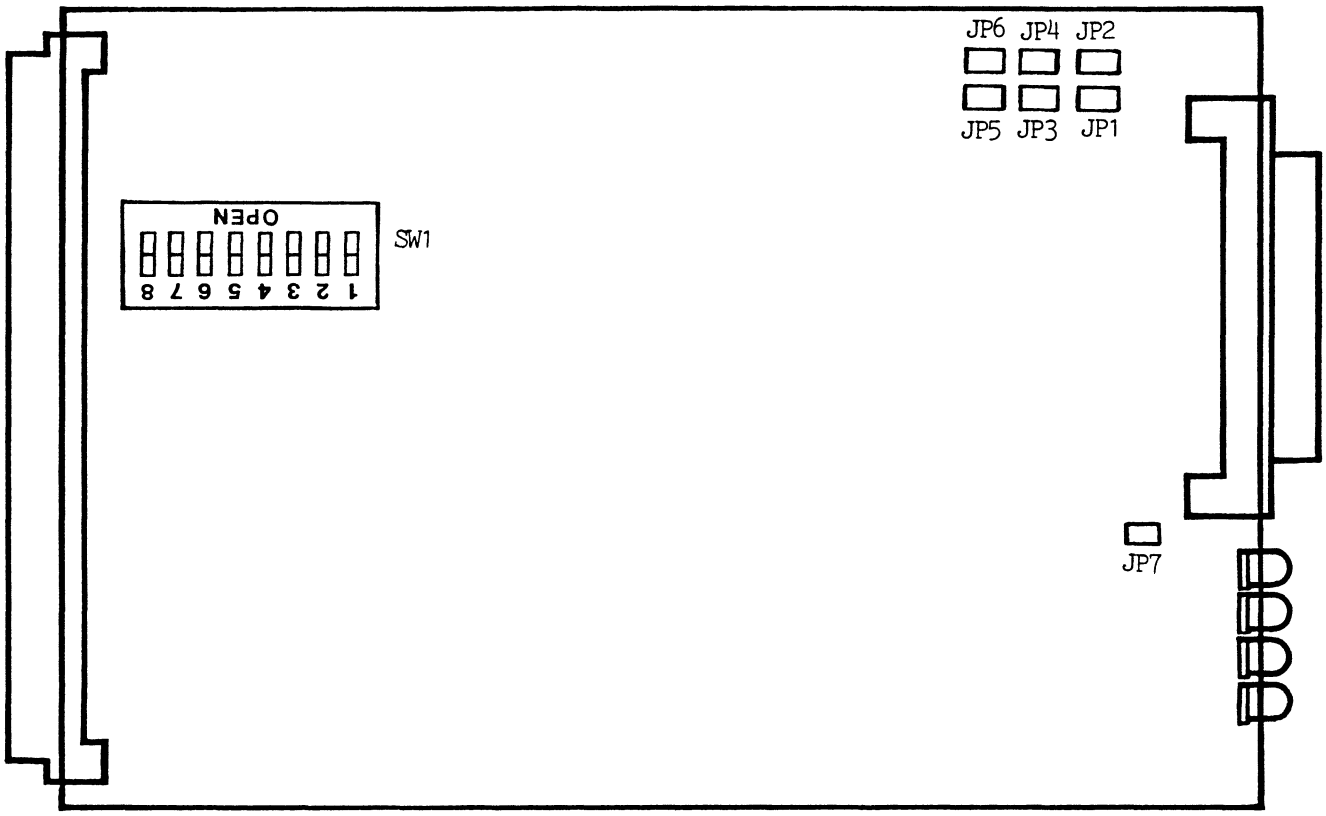
Table C-1 Default Settings

PARAMETER	SETTING
Channel 1 PPM	1
Channel 1 Range	1 (signed)
Channel 1 Position	0
Channel 1 Set Points	off
Channel 2 PPM	1
Channel 2 Range	1 (signed)
Channel 2 Position	0
Channel 2 Set Points	off

APPENDIX E

MODULE CONFIGURATION

Figure E-1 Module Configuration Worksheet
Dual Channel Incremental Encoder Interface



Settings		
SW1	CARD MAPPED TO SHORT ADDRESS:	
JP1, 2, 3	CHANNEL ONE ENABLED FOR:	☐ SINGLE-ENDED ENCODERS ☐ DIFFERENTIAL ENCODERS
JP4, 5, 6	CHANNEL TWO ENABLED FOR:	☐ SINGLE-ENDED ENCODERS ☐ DIFFERENTIAL ENCODERS
JP7	ENCODER POWER SET TO:	☐ +5VDC ☐ +12VDC